ID 810C: Renesas On-line Virtual Power Laboratory “Renesas VP”

Renesas Electronics America Inc.
Jim Comstock
Technical Marketing Manager
13 October 2010
Bio - Jim Comstock

Current Position:
- **Renesas Electronics America** - Manager, New Business Development and Technical Marketing - Power MOSFETs, DrMOS, POLs and Scalable VR’s Products

Technical Experience:
- 17+ Years - **Renesas Electronics America**, and **Hitachi America**
  - 8 Years - Siliconix, Inc.
  - 14 Years - Fairchild Camera and Instrument, Inc.
  - 6 years - Stanford Singer Research Laboratory
  - 4 Years - USAF – Non-Commissioned Officer – Japan & Korea Veteran
  - 4 Years - General Motors Apprenticeship
- 53+ Years total

Formal Education: 7 Full-time Years - Oregon State University: MSEE, BSEE, ++

Pats on the Back: >20

My Motto:
“Love what you do, plan, focus, work hard, maintain your integrity and the rewards will follow you!”
Renesas Technology and Solution Portfolio

Microcontrollers & Microprocessors
#1 Market share worldwide *

ASIC, ASSP & Memory
Advanced and proven technologies

Analog and Power Devices
#1 Market share in low-voltage MOSFET**

Solutions for Innovation

* MCU: 31% revenue basis from Gartner "Semiconductor Applications Worldwide Annual Market Share: Database" 25 March 2010
** Power MOSFET: 17.1% on unit basis from Marketing Eye 2009 (17.1% on unit basis).
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Renesas Power Management Devices and Solutions

Broad Product Lineup

- **Scalable Multi-SiP Solution**
  - Hybrid Analog/Digital VR control
  - Fully scalable, 2 rails up to 8 phase or 240A each
  - Super efficiency from 1% to 100% of full load
  - CPU & GPU for Server, Workstation, and NBPC

- **Compact and Integrated SiP**
  - 8x8 and 6x6 Package integrates PWM, Driver, HS+LS FET
  - Capable to 40A; peak efficiencies reach 94%
  - Networking/Computing main board 12 or 19Vin to 0.6 to 3Vout

- **Performance Package**
  - For best efficiency in high current applications
  - Up to 175°C and 180A Id
  - Industrial, Automotive, Telecom, DC-DC Module

- **Value Package**
  - Leadless, SO-8 footprint compatible Thin-Profile Package
  - Al Ribbon Bonding supported to lower package resistance and cost
  - PC/Server and Mobile Applications

- **Standard Package**
  - Industry-Standard Package
  - Low cost
  - General Purpose for non-isolated DC-DC

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Renesas Power Management Devices and Solutions: Scalable, Compact and Integrated SiPs

### Scalable Multi-SiP Solution
- Hybrid Analog/Digital VR control
- Fully scalable, 2 rails up to 8 phase or 240A each
- Super efficiency from 1% to 100% of full load
- CPU & GPU for Server, Workstation, and NBPC

### Compact and Integrated SiP
- 8x8 and 6x6 Package integrates PWM, Driver, HS+LS FET
- Capable to 40A; peak efficiencies reach 94%
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Renesas Power Management Devices and Solutions

Discrete Single and Dual MOSFETs

Scalable Multi-SiP Solution
- Scalable VR control
- Supports up to 8 phase or 240A each
- From 1% to 100% of full load
- Power, Workstation, and NBPC

Compact and Integrated SiP Performance Package
- Low cost
- General Purpose for non-isolated DC-DC

Performance Package
- For best efficiency in high current applications
- Up to 175°C and 180A Id
- Industrial, Automotive, Telecom, DC-DC Module

Value Package
- Leadless, SO-8 footprint compatible
- Thin-Profile Package
- AI Ribbon Bonding supported to lower package resistance and cost
- PC/Server and Mobile Applications

Standard Package
- Industry-Standard Package
- Low cost
- General Purpose for non-isolated DC-DC
Our Customer’s are constantly “Innovating” in their new Product Solutions!

All “Product Solutions” require “Design Innovations” to reduce:

1. Power Losses
2. Component Sizes & Count
3. BOM Costs

These “Reductions” are needed NOW!
Renesas’s Goals:
Increase the Efficiency and Reduce Size and Cost of our Customer’s Innovative Products!

Goal 1: Decrease the converters power losses from “AC Line to each load” by to increasing the “Total Efficiency” and reducing the “Components Size” and “Cost”.

Goal 2: Increase “Battery Operating Time” by increasing the Light and Heavy Load Efficiencies and by reducing the Components “Physical Size” and “Cost”.

Goal 3: Reduce the AC Line & Stand-by Power Losses

A Product Labeling now requires “Certification Test Approval”
To help Our Customers achieve these Goals
Renesas has Innovative Power Products

Discrete Lineups

DrMOS SiP Devices

POL SiP Devices

Next Gen. Discretes

Next Gen. Dr MOS SiPs

Next Gen. POLs

Scalable multi-phase VR.
Please attend the Renesas Presentation - 820C.
What is the Agenda for “Renesas VP”?

1. Define “Renesas VP”? What is it?

2. Describe VP’s “Registration” and “Log-on” Procedure.

3. Explain VP’s “Active Datasheet Library’s” features.

4. Explain VP’s “Buck Designer’s” features.

5. Show VP’s link to “Free” VP off-line simulation tools
Key **VP** Takeaways

A User in a few minutes will learn to:

1. **Generate** datasheet graphs dynamically using a User’s “Test Conditions”.

2. **Setup** a converter’s “Design Requirement’s”,

3. **Select** a “Renesas Recommended” HS & LS Renesas MOSFET pair, or

4. **Select** a “User’s Custom” HS & LS Renesas MOSFET pair,

5. **Generate** “Efficiency”, “Transient Waveforms” and AC “Bode” Plots,

6. **Document and Save** the design, and

7. **Download** Renesas VP’s “Free” on-line software.

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One “Internet Link” to Renesas VP

http://america.renesas.com/products/discrete/power_mos/vp/vp_landing.jsp

1. Bookmark this link.

The Fast Link to VP

VP’s Start Page

2. Click here to download the “System Overview” and the “Renesas VP User” Manuals.

4. Registered User

3. New User
VP’s “Log-in” Screen

Renesas Lab. VP

Important Notice
Renesas Electronics Corporation was established on 1 April 2010. If you had an account at the former Renesas Technology or NEC Electronics Web sites, you can login to the Renesas Electronics site using the same email address and password. If you cannot login, please reset your password.

Renesas Electronics Corporation looks forward to continuing to serve you in the future.

Login

Please login to proceed the process.

Email address
Password

Forgot your password?

New user? Click here to register now

Enter Your Email address.
Enter Your Password.
VP’s “Landing Page” after Logging-in

1. “Active Datasheet Library”

2. “Buck Designer”

ACTIVE DATASHEET

Renesas provided Active Datasheets, that contain graphical charts of essential characteristics.

Reverse Output Characteristics
Typical Output Characteristics
Dynamic Input Characteristics
Transfer Characteristic
Switching Test (Pulse testing supported)
Capacitance Test
RDSon Test

GO TO ACTIVE DATASHEET LIBRARY

BUCK DESIGNER

The Buck Designer facilitates a customers buck converter design before the evaluation board.

Efficiency Calculation with Renesas FETs and given parameters can be achieved without an actual evaluation board. (Result are calculated with default parameters and you can also calculate them your own parameters, so that you can learn which parameter affects the characteristics your interested in.)

Recommendation list: Default simulations by Renesas recommend combinations of Low-side and High-side FETs.

FET selection: Simulation done with Customer selected FETs, customized conditions and parameters.

GO TO BUCK DESIGNER
What is the “Active Datasheet Library”? 

VP’s 
“Active Datasheet Library”
Key Features of VP’s “Active Datasheet Library”

1. Let’s the User download a Renesas static PDF datasheet.

2. It can display up to 10 nominal datasheet graphs for a User’s selected Renesas MOSFET.

3. It Allows a User to enter “Custom” test conditions and graph the behavior of up to 10 selected Renesas Focus MOSFET graphs, in a few minutes, without the need for extensive laboratory bench testing.
Now return to VP’s “Landing Page” and Go To the “Active Datasheet Library”

Select the Library

“Active Datasheet Library”

Click Here
This is **VP’s “Active Datasheet Library”** List of Renesas Focus MOSFETs

1. Note the column headings.

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Active Datasheet</th>
<th>Package</th>
<th>ID (A)</th>
<th>$V_{DSS}$ (V)</th>
<th>$R_{DS(ON)}$ @10V (mΩ)</th>
<th>$R_{DS(ON)}$ @4.5V (mΩ)</th>
<th>$C_{ISS}$ (pF)</th>
<th>Recommend</th>
<th>Static Datasheets</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJK0331DPB</td>
<td>Select</td>
<td>LFPAK</td>
<td>40</td>
<td>30</td>
<td>3.4</td>
<td>4.9</td>
<td>3380</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0332DPB</td>
<td>Select</td>
<td>LFPAK</td>
<td>35</td>
<td>20</td>
<td>4.7</td>
<td>7</td>
<td>2180</td>
<td>High-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0346DPA</td>
<td>Select</td>
<td>WPAK</td>
<td>65</td>
<td>30</td>
<td>2</td>
<td>2.7</td>
<td>7650</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0348DPA</td>
<td>Select</td>
<td>WPAK</td>
<td>60</td>
<td>30</td>
<td>2</td>
<td>2.7</td>
<td>7650</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0348DPA</td>
<td>Select</td>
<td>WPAK</td>
<td>60</td>
<td>30</td>
<td>2</td>
<td>2.7</td>
<td>7650</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
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<td>Select</td>
<td>WPAK</td>
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<td>30</td>
<td>2</td>
<td>2.7</td>
<td>7650</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0349DSP</td>
<td>Select</td>
<td>SOP-8</td>
<td>18</td>
<td>30</td>
<td>5.2</td>
<td>6.9</td>
<td>2560</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0351DPA</td>
<td>Select</td>
<td>SOP-8</td>
<td>20</td>
<td>30</td>
<td>5.2</td>
<td>6.9</td>
<td>2560</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0351DSP</td>
<td>Select</td>
<td>SOP-8</td>
<td>20</td>
<td>30</td>
<td>5.2</td>
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<td>PDF</td>
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<tr>
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<td>Select</td>
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<tr>
<td>RJK0353DPA</td>
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<td>Low-side</td>
<td>PDF</td>
</tr>
<tr>
<td>RJK0353DSP</td>
<td>Select</td>
<td>WPAK</td>
<td>35</td>
<td>30</td>
<td>5.2</td>
<td>6.9</td>
<td>2560</td>
<td>Low-side</td>
<td>PDF</td>
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<tr>
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<td>WPAK</td>
<td>35</td>
<td>30</td>
<td>5.2</td>
<td>6.9</td>
<td>2560</td>
<td>Low-side</td>
<td>PDF</td>
</tr>
</tbody>
</table>

2. The User can Scroll the List to view the MOSFETs in Renesas’s “Active Datasheet Library” and decide upon a MOSFET that the User wanted to “Select” for further study.

3. The User decided on the RJK0346DPA MOSFET.

4. Download the *.pdf datasheet.

5. Then, click “Select” and the display will “Go To” the selected MOSFET’s “Starting Page”.

Scroll up/down to see more MOSFETs listed in the Library.
1. This is the MOSFET part number and brief description of the MOSFET that was selected by the User from the ”Active Datasheet Library”.

2. Click here to download and view the PDF Static Datasheet if you do not have it already.

3. Click here to download the Spice Model if you want it.

4. This is a list of 10 stand alone “Active Datasheet” graph “Labels” and a “Summary Display” that includes all of the 10 graph Labels.

5. These are all Typical test conditions if the User DOES NOT “Edit” at this point in time.

6. Click here to “Run All Tests” for ALL 10 of the “Active Datasheet’s” Typical graphs.

7. The 1st of the 10 “Active Datasheet Graphs” “TYPICAL OUTPUT” will appear here when the simulations are finished.
Clarifications are needed regarding the “Active Datasheet’s” graph’s “Labels” and the displayed graph’s “Variables”

The Renesas MOSFET “Active Datasheet” Tool can generate dynamically 10 different datasheet graphs, using a “User’s specified” test conditions.

**VP’s Graph’s “Labels”**

1. Summary  
2. Typical Output  
3. Transfer  
4. Vdson vs. Vgs  
5. Rdson vs. Ids  
6. Rdson vs. Temperature  
7. Capacitance  
8. Dynamic Input  
9. Reverse Output  
10. Rdson vs. Vgs  
11. Switching Characteristic

**VP’s Graph “Variables”**

(Displays all 10 Graphs #2 to #11)
- Id vs. Vds and Vgs  
- Id vs. Vgs and Temperature  
- Vdson vs. Vgs and Ids  
- Rdson vs. Ids and Vgs  
- Rdson vs. Tcase and Vgs  
- Ciss, Coss, Crss vs. Vds  
- Vgs vs. Charge and Vds  
- Idr vs. Vsd and Vgs  
- Rdson vs. Vgs and Temperature  
- Vds & Vgs vs. Time

**Note:** A “User’s specified” graph test result's must be used in conjunction with the other important and related MOSFET datasheet parameters that are included in the static PDF datasheet.
After “Running All Tests” the “Typical Output” Labeled Graph Appears

1. After “Clicking” on “Run All Tests”, a “Summary” for each of the 10 “Analysis” labels will be generated and will appear in sequential ascending order for the selected MOSFET (in this case the RJK0346DPA).

2. The first displayed graph is the “Typical Output Characteristics” graph.

3. Test Parameters

4. Ids Current

5. Vds Voltage

6. Vgs

7. Click “Edit” here on any of the 10 graphs if you want to change their “Test Conditions” or View the “Test Circuit”.

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This is the “Rdson vs. Temperature” Labeled Graph

1. Select the RJK0346 DPA from the Active Datasheet List to “Go To the Starting Page.”
2. Click “Edit” here to Edit the graph if you want to change the “Test Conditions” or View the “Test Circuit”.
3. Click “Edit” here to Edit the graph if you want to change the “Test Conditions” or View the “Test Circuit”.

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This is the “Dynamic Input” Labeled Graph “Vgs vs. Charge”

1. Select the RJK 0346 DPA from the Active Datasheet List to “Go To the Starting Page”.

2. Click “Edit” here to Edit the graph if you want to change the “Test Conditions” or View the “Test Circuit”.

3. Click “Edit” here to Edit the graph if you want to change the “Test Conditions” or View the “Test Circuit”.
This is the “Edit” Screen for the RJK0346DPA’s “Typical Output” Test Parameters

1. User “Clicked” on “Edit” under the displayed “Configuration Table” to the right of the “Typical Output” graph.

2. The “Test Circuit” is displayed.

3. If desired, a User can change these 4 test parameters and then click “Run Test” to run the test using the new test “Configuration” values.

4. When the new “Run Test” is completed, a new graph is generated showing the effect of the test configuration’s changes.

5. This “Edit” procedure applies to all 10 of the graph labels.
Let Us Review VP’s “Active Datasheet Library”

1. VP’s listing of “Renesas’s Focus MOSFETs” was obtained.
2. Download links to VP’s Static Datasheets and Spice Models for each Renesas Focus MOSFET was shown.
3. VP’s “Active Data Sheet Library” allows a User to display 10 nominal static datasheet’s graphs for each Renesas Focus MOSFET in the library.
4. Competitive Vendor’s static datasheets do not normally use the same static datasheet test conditions for their datasheet graphs.
5. VP allows the User to “Edit” an “Active Datasheet Library’s” datasheet test conditions and dynamically generate new graphs.
6. Now, let us “Change the Topic” and transition to VP’s “Buck Designer” and review it’s Purpose and Features.
What is VP’s “Buck Designer”?
VP’s “Buck Designer” is used for designing a “Synchronous-Buck” Converter.

This is a “Synchronous-Buck” Converter.
Features of VP’s “Buck Designer”

When using Renesas VP a User can:

1. Specify:
   • System “Design Requirements”
   • System “Advanced Requirements”

2. Select Renesas HS & LS MOSFET Pairs:
   • From a “Renesas Recommended MOSFET Pair List”, or
   • By the User doing a “Custom Selection” from the Renesas MOSFET Library List.

3. Simulate and Display quickly the:
   • “Efficiency” Graphs
   • “Transient” Waveforms
   • AC “Bode” Plots

4. Change passive component values and re-simulate, if needed.

5. Review, Print and Save a “Design Summary Report”:

6. Save the design on-line in VP’s “My Design”.

7. Download “Free” VP off-line design software.
Now Return to VP’s “Landing Page”

1. Go back to the “Landing Page”.

2. “Buck Designer”

3. Click Here
This is VP’s “Design Requirements” Screen

1. The User must enter 8 mandatory “Design Requirements” for the User’s design.

2. This is a User’s “Reference Name” for the application.

3. The User clicks here to Show or Hide the “Advanced Requirements” Entry Table.

<table>
<thead>
<tr>
<th>Requirements</th>
<th>Design Requirements</th>
<th>Advanced Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Vin</td>
<td></td>
</tr>
<tr>
<td>VOUT</td>
<td>Vout</td>
<td></td>
</tr>
<tr>
<td>IOUTMAX</td>
<td>Ioutmax</td>
<td></td>
</tr>
<tr>
<td>FS</td>
<td>Fs</td>
<td></td>
</tr>
<tr>
<td>VGSDR</td>
<td>Vgsdr</td>
<td></td>
</tr>
<tr>
<td># PHASES</td>
<td># Phases</td>
<td></td>
</tr>
<tr>
<td>TEMPERATURE</td>
<td>Ta</td>
<td></td>
</tr>
<tr>
<td>LOUT</td>
<td>Lout</td>
<td></td>
</tr>
<tr>
<td>APPLICATION</td>
<td>Application</td>
<td></td>
</tr>
</tbody>
</table>
This is VP’s “Advanced Requirements” Screen

1. This screen is located directly below the “Design Requirements” Screen.

2. Enter the 9 required “Advanced Requirements”.
   - Lout esr
   - Cbulk
   - Cbulk esr
   - Chfcap
   - Chfcap esr
   - Linput
   - Linput esr
   - Cinput
   - Cinput esr

3. Click here to “Hide” the “Advanced Requirements” screen, if you desire. Then, GO BACK again to the “Design Requirements” screen located above this screen.
The User returned to VP’s “Design Requirements” Screen

1. The user now clicks “Next” to GO TO the listing of the “Renesas Recommended HS & LS MOSFET Pairs” combinations screen.
VP’s “Renesas Recommended” or “Custom Solutions” Selection Screen

1. The User first selects the “Recommended Solutions” tab and reviews the specific information for each HS & LS “Renesas Recommended Pair” combination.

2. The User reviewed the “Recommended Pair Listing” and decided to study this recommended pair – the RJK0332DPB and the RJK03C2DPB.

3. The user then clicks “Select” to start the analysis procedure and it goes to the “Schematics and Efficiency” screen.
This is VP’s “Schematics & Efficiency” Sheet

1. Click here and the “Switching Circuit Schematic” appears.

2. Note: Any “blue” colored passive component can be changed.
   If a User wants to change the MOSFETs, then the User will have to return to the previous screen and re-select them and then return to this screen.

3. Click here to generate the “Efficiency” Graph that is shown on the next slide.
VP generated the “Efficiency vs. Iout Graph” for the User’s Selection from the “Renesas Recommended MOSFET Pair List”

Selected MOSFET Pair: RJK0332DPBx1 and the RJK03C1DPBx1

Result is calculated with given Tch and if calculated dissipation can’t be ignored, try again with Tch raising of heat resistance multiple calculated dissipation.
VP can also generate “Switching Waveforms” for the “Renesas Recommended MOSFET Pair”

1. Go back to the “Schematic’s and Efficiency Calculation Page. Click “Switching Circuit” and then Click “Start Simulation”.

2. These 3 Results Buttons will appear when the simulation is finished.

3. Click “Switching” to display the VLOUT & ILOUT “Switching Waveforms”.
VP generated the waveforms for “VLOUT” Node and the “Inductor Current, ILOUT” for the “Renesas Selected” MOSFET Pair.

Selected MOSFET Pair: RJK0332DPBx1 and the RJK03C1DPAx1
4-4. Operation of Viewer

- Drag: Move the waveform according to the mouse movement in zoomed mode.
- [Zoom In]: Enlarges the waveform displayed stepwise by x%.
- [Zoom Out]: Shrinks the waveform displayed stepwise by x%.
- [Marquee Zoom]: Enlarges the waveform in the selected area to the full size of the screen (area zoom
- [Go back one zoom level]: Go back one zoomed level.
- [Go forward one zoom level]: Go forward one zoomed level.
- [Reset Zoom]: Reset the zoomed mode to its default.
- [Print Waveforms]: Print the waveforms.

Move the position of [M1] and [M2] with dragging vertical lines.

Move a selected waveform up. (*)
Move a selected waveform down. (*)
Select all waveforms.
Deselect all waveforms.
* Click an item name to select.

Display the values of [M1] and [M2].

Use functions such as RSM, average and peak values.

Checking or un-checking the checkbox in front of the waveform name will turn the display on or off.
A User can also do a **VP “Custom Solution”** by selecting the HS & LS MOSFETs from the Renesas “Custom Solutions Lists”

1. A User Selects High-side and Low-side MOSFETs from these two lists of Renesas “Custom Solutions” recommended MOSFETs.

2. Select HS MOSFET

3. Set Qty

4. Select LS MOSFET

5. Set Qty

6. The User can “Calculate” the “Power Loss” for any selected MOSFET combination until the User is satisfied with the power loss (Refer to the next slide).

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For each of User’s “Custom Solution” Trials, VP records the “Total Loss”

1. For each new User Trial MOSFET Combination, click “Calculate” and the Total Loss for each trial combination will be recorded as shown above.

   The User can then select, at any time, any one of the recorded trial combinations to “Analyze” further.

2. The User performed 3 trials and the “Total Loss” for each trial combination was listed.

3. The User selected this “Trial Combination” to “Analyze”.

VP’s generated “Efficiency vs. Iout” Graph for the User’s “Custom Solution”

Selected MOSFET Pair: RJK0305DPBx1 and the RJK0328DPBx1

Result is calculated with given Tch and if calculated dissipation can’t be ignored, try again with Tch raising of heat resistance multiple calculated dissipation.
VP's generated waveforms for "VPHASE" and the "Inductor Current, IOUT" for the User's "Custom Solution"
VP can also generate AC “Bode” Plots

1. Click the “System Schematic”

2. To do a “BODE Plot” simulation, GoTo the System Schematic and Set “Select Analysis” to “AC”.

3. Click “Configure” and enter the “Start and Stop Frequencies”.

4. Click “GO”.

5. Click “Start Simulation” to start generating the BODE Plot.

6. You will have to wait a while until the “BODE Plot’s” blue display “Button” appears here. Then, Click on it!
VP generated the “Bode” Plot

Selected MOSFET Pair: RJK0332DPBx1 and the RJK03C1DPBx1
VP generates a “Design Summary Report”

1. This is the first item in the User’s “Design Summary” Report.

2. These are the User’s Selected MOSFETs.

3. You can scroll down & up the report.

4. The “Design Summary” *.pdf file can be downloaded.

5. A User can save the design on-line by clicking on “My Designs”.

6. A “Free” off-line software “Download Link” is located at the bottom of the “Design Summary Listing“. 
VP includes “Free” Off-line Simulation Tools

1. For users with restricted access to simulation technology, “Renesas VP Off-line” provides a free full featured simulation package to users of Renesas VP.

2. The free package can be downloaded, installed, and configured on a User’s computer ready for immediate off-line VP analysis.

3. The download link for the free software is located at the end of the “Design Summary Sheet” and is displayed there as:

Click Here!
Concluding Comments

1. The purpose of the presentation was to provide a Quick Start Demonstration of VP’s two on-line tool’s: 1) The “Active Datasheet Library” and 2) The “Buck Designer”.

2. One main goal of Renesas VP is to allow a User to quickly obtain initial Efficiency and Switch Node Waveforms, when evaluating using Renesas MOSFETs, in a few minutes without performing initial time consuming and labor intensive “Bench” testing.

3. VP Users can select Renesas MOSFETs for a converter design by using:
   a) “VP’s recommended HS & LS Renesas MOSFET pair combinations” or a
   b) “User’s Custom Pair Selection” of Renesas MOSFETs from the Library,

4. The best way for a User to learn Renesas VP’s features, is to go “on-line” and use the program in real time.

5. The program’s operational details are available for download on-line in the “Renesas VP Brochure” and the “Renesas VP User’s Manual”.
   (http://america.renesas.com/products/discrete/power_mos/vp/vp_landing.jsp)

6. This presentation was “NOT” aimed to teach a User how to design and/or optimize a Synchronous-Buck converter. This complex topic will be reviewed in a future Renesas presentation.
One Last Comment!

Our Customer’s are constantly “Innovating” in their new Product Solutions!

The “New Customer Solutions” require “Design Innovations” to reduce:

1. Power Losses,
2. Component Sizes & Count, and
3. BOM Cost

Renesas Electronics America can help “YOU” meet these “Goals” -- TODAY!
Questions?
Thank You All for Attending DevCon!