Insights into MCU & Mixed Signal Design

Bartt Richards, Principal Design Engineer
Joshua Lawton, Sr. Staff Engineer
w/ Keith Larson, Senior Marketing Manager
Bartt Richards: Principal Design Engineer

Education
- BSEE: Duke University 1988
- MSEE: NC State University 1995

24 Years Semiconductor Industry Experience
- 10½ Yrs: Mitsubishi Semiconductor America
  - 8 and 16-bit MCU Design Engineer (740 and M16C)
- 11 Yrs: NEC Electronics America
  - 8 and 32-bit MCU Design Manager (78K and V850E)
- 2½ Yrs: Renesas Electronics America
  - 32-bit MCU System Design Engineer (V850E)
Keith Larson: Senior Marketing Manager

Education
- BSET: Purdue University, December 1990
- MEng: Cornell University, May 1996
  - Emphasis in Control Systems and Computer Architecture

Experience
  - 5 years in Manufacturing Engineering, Test Development, Circuit Development
  - 12 years in IC Architecture and Development
    - IC specification and requirements development, evaluation
    - Circuit development and simulation, analysis, IC design support
    - Powertrain, braking, crash-sensing, networking and body ECU expertise
- Renesas Electronics America Inc. (2008 +)
  - Senior Marketing Manager for Analog and Power Products
  - Mixed-signal market development for North America
Renesas Technology & Solution Portfolio
**Microcontroller and Microprocessor Line-up**

### 2010

- **1200 DMIPS, Superscalar**
  - Automotive & Industrial, 65nm
  - 600µA/MHz, 1.5µA standby

- **500 DMIPS, Low Power**
  - Automotive & Industrial, 90nm
  - 600µA/MHz, 1.5µA standby

- **165 DMIPS, FPU, DSC**
  - Industrial, 90nm
  - 200µA/MHz, 1.6µA deep standby

- **25 DMIPS, Low Power**
  - Industrial & Automotive, 150nm
  - 190µA/MHz, 0.3µA standby

- **10 DMIPS, Capacitive Touch**
  - Industrial & Automotive, 130nm
  - 350µA/MHz, 1µA standby

### 2012

- **1200 DMIPS, Performance**
  - Automotive, 40nm
  - 500µA/MHz, 35µA deep standby

- **165 DMIPS, FPU, DSC**
  - Industrial, 40nm
  - 200µA/MHz, 0.3µA deep standby

- **Embedded Security, ASSP**
  - Industrial, 90nm
  - 1mA/MHz, 100µA standby

- **44 DMIPS, True Low Power**
  - Industrial & Automotive, 130nm
  - 144µA/MHz, 0.2µA standby
‘Enabling The Smart Society’

Challenge:
“Ever increasing automotive requirements result in the demand to integrate complex MCU and Mixed Signal devices with features that are seemingly impossible to realize. What steps can be taken during development to achieve the unattainable?”

Solution:
“This class will introduce complexities dealt with during MCU and Mixed Signal development and the design steps taken to address some of these difficult automotive requirements.”
Agenda: MCU

- MCU Introduction
- Development Flow
  - Specification
  - Front-End
  - Back-End
- Challenges during development
- Automotive Requirement: Power Reduction
  - Power modes
  - Power switches
  - Power domains
MCU Development:

WHAT OUR SALES PEOPLE THINK WE DO
MCU Development:

WHAT OUR SALES PEOPLE TELL OUR CUSTOMERS WE DO
MCU Development:

WHAT WE THINK WE DO
MCU Development:

WHAT WE ACTUALLY DO

```c
/**
 * Chip Select Decoder
 */

always @(address or PSEL)
    begin
        if (PSEL)
            begin
                PSEL_SCC1_I0_CSDECP_I004 <= 1'b0;
            end
            address >= 32'hFF426000 && address <= 32'hFF426003
                begin
                    SCC1_I0_CSDECP_I004 <= 1'b1;
                end
                address >= 32'hFF426050 && address <= 32'hFF426053
                begin
                    SCC1_I0_CSDECP_I004 <= 1'b1;
                end
            address >= 32'hFF426060 && address <= 32'hFF426063
                begin
                    SCC1_I0_CSDECP_I004 <= 1'b1;
                end
            address >= 32'hFF426070 && address <= 32'hFF426073
                begin
                    SCC1_I0_CSDECP_I004 <= 1'b1;
                end
            address >= 32'hFF426090 && address <= 32'hFF426093
                begin
                    DECP_I004 <= 1'b1;
                end
            address >= 32'hFF4260A0 && address <= 32'hFF4260A3
                begin
                    DECP_I004 <= 1'b1;
                end
        end
```
**MCU = Micro-Controller Unit**

- **1 x Timer Array Unit** (1 x 16ch TAUJA)
- **1 x OSTM**
- **Window Watchdog**
- **2 x CSI**
- **3 x CSI with FIFO**
- **4 x I²C**
- **5 x UART**
  - LIN compatible
- **5 x Multi LIN Master**
- **4 x I²S**
- **2 x PCM**

**Package: 144pin QFP**

**32-bit CPU**
- 160 MHz operation
- I/O : 3.0 – 3.6 V
- Internal : 1.1 - 1.3V
- -40 to +85C / +105C

**Memory**
- 2MB CODE FLASH (ROM)
- 64KB Local RAM
- 32KB Data Flash

**A/D Converter**
- 16ch / 10-bit
- On-Chip Debug

**External bus I/F**
- (SRAM&SDRAM)
- PLL & SSCG

**System Protection Function**
- 16 x DMA

**Stand-by Control**
- 1 x Timer Array Unit (1 x 4ch TAUJ)
- RTC (Watch Timer)
- Window Watchdog
- Key Return
- Main OSC
  - 4 to 20MHZ
- Internal OSC
  - 240kHz + 8MHZ
- SubClk
  - 32kHz

- **2 x aFCAN**
  - (2 x 64msg aFCAN)

- **MLB**
- **IE Bus**
MCU Development Flow
MCU Development Flow:

**Requirements**
- Customer Input
- Market Input

**Spec**
- System Design Information

**Front-End**
- Creation of NETLIST from Specification
  - Design Libraries
  - Macros

**Back-End**
- Creation of Layout Data (Mask Data) from NETLIST

**Mask Data**
Specification Creation:

Information for Design (FE and BE)

Information for User's Manual creation

Information for Test Development

Information for Tools Development

Table 3.1.2. Main Mode

<table>
<thead>
<tr>
<th>Signals</th>
<th>Description</th>
<th>TAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>Single Chip Mode (SU)</td>
<td>RCUUTAP</td>
</tr>
<tr>
<td>0 1</td>
<td>Setting prohibited</td>
<td>YES (Setting prohibited)</td>
</tr>
<tr>
<td>1 0</td>
<td>Flash Writer Mode (FD)</td>
<td>RCUUTAP</td>
</tr>
<tr>
<td>1 1</td>
<td>Test Mode</td>
<td>MODE2=0: LVTAP, MODE1=1: RCUUTAP</td>
</tr>
</tbody>
</table>

(1) This setting is only disclosed to the crystal manufacturer for characterization of the crystal.

(2) Use pull-down resistance to PD. Also, do not input high level to PD-1 till the start of user's program.
Front-End Development:

- **NETLIST**: ASCII representation of entire device used for functional verification, timing verification, physical layout tools.
- **Verification**: Confirm that NETLIST functionality meets system specification; confirm that timing specification can be met.
- **Test Pattern Generation**: based on functional simulation, generate patterns to be used for qualification and mass production testing.
Back-End Development:

Floor plan: placement of hard macros and I/O
I/O Ring development
Power Grid
Place/route soft macros

Physical Verification (DRC/LVS)
Design For Test insertion

ONE KEY GOAL:
*Reduce Size = Reduce Cost!*

**Hard Macro:** process-specific circuit with fixed physical dimension and layout

**Soft Macro:** process-independent circuit; physical placement modified to match floorplan requirements
Challenges Along the Way...
Complexities of Functional Integration

- Feature Reduction:
  - Memory Size
  - Macro reduction

- Pin Function Assignment:
  - Multiplex functions
  - Power/Ground pair requirements

- Clocking/Reset Assignment:
  - Macro clock selection
  - Clock and reset synchronization
Pin Function Assignment

- Power/Ground pair requirements
- Multiplex functions

- How many core pair required?
- How many I/O pair required?
- Function specific power pairs required?
- Application feasibility?
- Design feasibility?
- Timing feasibility (cross-chip timing)?
Clock Distribution

- Macro clock selection
- Clock and reset synchronization

**Diagram:**
- PLL for adjusting clock rates
- Flash ROM and RAM with low and high-performance buses
- Clock divider for managing clock frequencies
- Reset sync for timing synchronization
- Port and macro function I/O connections
FRONT END: Timing Closure

**ON-CHIP TIMING**

Static Timing Analysis:
- Hold violations
- Setup violations

Clock Tree Synthesis:
- Clock skew

**OFF-CHIP TIMING**

Application Timing Requirements:
- Off-chip delays
- Round-trip timing
Static Timing Analysis (STA)

- $t_{SU} = \text{setup time}$
- $t_H = \text{hold time}$
- $t_D = \text{delay time}$

How many setup and hold checks are we talking about???

MILLIONS!
Clock Skew

CTS = CLOCK TREE SYNTHESIS
Application Timing

- Off-chip Delays:
  - a. Capacitive load
  - b. Size of buffer

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Condition</th>
<th>Spec</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IISAnWS (output) Duty Cycle</td>
<td></td>
<td></td>
<td>MIN.</td>
<td>TYP.</td>
</tr>
<tr>
<td>IISAnSCK Edge to IISAnWS output delay time</td>
<td>t_WSOD</td>
<td></td>
<td>45</td>
<td>55</td>
</tr>
<tr>
<td>IISAnSCK Edge to IISAnWS output hold time</td>
<td>t_WSODH</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>IISAnSCK clock period</td>
<td>T</td>
<td></td>
<td>140</td>
<td></td>
</tr>
<tr>
<td>IISAnSCK clock low-level width</td>
<td>t_SCKL</td>
<td></td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>IISAnSCK clock high-level width</td>
<td>t_SCKH</td>
<td></td>
<td>65</td>
<td></td>
</tr>
<tr>
<td>IISAnSCK Edge to IISAnSDO output delay time</td>
<td>t_SDOO</td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>IISAnSCK Edge to IISAnSDO output hold time</td>
<td>t_SDOH</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>IISAnSDI Edge to IISAnSCK falling Setup</td>
<td>t_SDIS</td>
<td></td>
<td>45</td>
<td></td>
</tr>
<tr>
<td>IISAnSDI Edge to IISAnSCK falling Hold</td>
<td>t_SDISH</td>
<td></td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

- Round Trip Timing: External DRAM example (READ)
BACK END: Physical Constraints and Concerns

- **Routing Congestion:**
  - Hard macro/Soft macro ratio
  - Impact to signal timing
  - Impact to chip size

- **Size Minimization:**
  - I/O defined or Core defined?
  - Aspect ratio decisions

- **Packaging Rules:**
  - Wire bonding & I/O location
PACKAGING: Wire Bonding Issues

- Wire length
- Wire angles
- Double bonding
- Non-connected pads
Power Reduction
Power Reduction

- Leakage current at small geometries:
  - Temperature effects
  - Transistor speed

- Power/Standby Modes:
  - Power/clock control
  - Transitioning between modes

- Power Domains:
  - On-chip power switches
  - Signals crossing boundaries
Power Mode Transitioning

- **Power ON**
- **Power OFF**

- **Reset**
  - AWO Iso0 Iso1

- **Run mode (ISO1 DeepStop)**
  - AWO Iso0 Iso1

- **HALT mode (ISO1 DeepStop)**
  - AWO Iso0 Iso1

- **Run mode (ISO1 Stop)**
  - AWO Iso0 Iso1

- **HALT mode**
  - AWO Iso0 Iso1

- **Stop mode (ISO1 DeepStop)**
  - AWO Iso0 Iso1

- **DeepStop mode**
  - AWO Iso0 Iso1

- **Stop mode**
  - AWO Iso0 Iso1
Power Switches

- On-chip power switches:
  - Many switches needed
  - Switches reduce usable area
  - Must be timed during power sequencing
Power Domains and Boundaries

- Signals crossing boundaries:
  - Every signal that crosses from one power domain to another must have masking logic in the event of power domain shut-off.
Agenda: Mixed Signal

- The Automotive Environment

- Mixed-signal Semiconductor Golden Rules
  - Accuracy & matching
  - Limitations

- Low-side Driver Circuit Design Example
  - Basic functionality
  - EMI
  - Protection
  - Detection
  - Quality
The Automotive Environment
Dealing with a Wide Voltage Range

Bus Lines
- Reverse Battery
- NOP
- Start
- Stop
- Normal Operation
- Double Battery
- Load Dump
- Bootstrap + Special Applications

Alternator Output Voltage vs. Temp

Alternator Ripple

Battery Voltage as a Function of Car Speed

Alternator Ripple Voltage (V)

Car speed

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Many More Challenges...

- Temperature Range
- Electro Magnetic Interference (EMI)
  - Immunity
  - Emissions
- Electro Static Discharge (ESD)
  - 2kV HBM minimum for all pins
  - 4kV signal lines leaving ECU
  - 6-8kV communications bus lines
Mixed-signal Semiconductor Golden Rules
Accuracy & Matching

In a semiconductor process the absolute value of parameters varies significantly...but the same devices match very well

Two Golden Rules of IC design:

- Do not rely on absolute tolerances (poor accuracy)
  - Resistors typically $\pm 20\%$
  - Capacitors typically $\pm 10\%$
  - $\beta$, $\mu_{N/P}$ typically $\pm 30\%$

- Rely on component matching
  - 0.1% is possible
  - Ratio design techniques using unit devices
  - Matched layout techniques
Limitations

Every device component has limitations

- **VGS**: < 4.0 (3.3V), < 7.0 (5V), < 7.0 (45V)
- **VDS**: < 4.0 (3.3V), < 7.0 (5V), < 45.0 (45V)
- **Matching**: ++ (3.3V), + (5V), - (45V)
- **Leakage**: ++ (3.3V), ++ (5V), - (45V)
- **Area**: (3.3V), (5V), (45V)
Achieving High Quality Starts at the Beginning!

- Design and system-level Failure Mode Effects Analysis (FMEA)

- **Design For Test (DFT)**
  - Automatic Test Pattern Generation (ATPG)
  - Full scan path for optimal test coverage
  - Logic supply quiescent current (IDDQ)
  - SHort Voltage Elevation (SHOVE)
  - Gate stress tests

- **Six-sigma Design**
  - Corner simulation (process, temperature, supply, load)
  - Monte-Carlo simulation
  - Allows Part Average Testing (PAT) and outlier screening

- **Others**
  - Design reuse
  - Expert reviews
Low-side Driver Circuit Design Example
Circuit Design

Let’s look at the design of a low-side driver

Step-by-step:
- Basic functionality
- EMI
- Protection
- Detection
- Quality
Basic Functionality

- Turn on/off lowside driver

Positive Supply Voltage

Input Threshold Detection

Digital Input Control Pin

Gate Drive Stage

Supply Reference Voltage

Low-side Driver Output

Power MOSFET Output Stage
Test Bench

1. Driver block from previous page
2. Power supplies (5V and 12V)
3. Control input
4. Application Circuitry
5. Wiring inductance
6. EMI Simulation
Basic Functionality

Issues?  **YES**

High peak current caused by charging the EMI capacitor

M69: 955.36942us 31.269322mA
Basic Functionality Issues - Zoom

- Fast turn-on creates a high current ($I = C \frac{dV}{dt}$)
- Current spike causes EMI issues
Basic + EMI

- Charge/discharge gate with a small constant current
  - Reduces slew rate which improves EMI
  1. Original control circuit
  2. Add current mirrors
Basic + EMI
EMC Improvement - CISPR25 Class 5 limit

New circuit passes CISPR25 class 5

Old circuit CISPR25 class 2 only!
Basic + EMI + Short Circuit Protection

- Short to battery will create a high current limited only by the on resistance of the output driver

Add current limitation circuit
1. Current sense
2. Voltage reference
3. Control amplifier (constant current output)

Control switching
4. Current mirror
5. Control switches
Basic + EMI + Short Circuit Protection Simulation Results

- Normal load
  - Without Current Limit (No self heating)
- Short to battery

**Increased output current**
- M1: 899.58427mA 31.272328mA
- M2: 2.8266122ms 399.95747mA

**Decreased gate drive voltage**
Basic + EMI + Short Circuit Protection
System considerations

Power dissipation in a short circuit condition is too high for the device in many cases.

Power dissipation can be handled by:

- Thermal shutdown
  - Auto restart for a x number of cycles before latching off
- Over-current detection and shut-down
  - Short detection debounce to limit temperature increase

Fast thermal transients > 60°C will reduce the lifetime of the part.
Basic + EMI + Short Circuit Protection + ESD

- +/- 4kV HBM applied at out pin
  - Positive ESD - Add gate trigger structure
  - Negative ESD - Use body diode of power transistor

1. Gate trigger
2. Gate charge current block
3. Gate source protection
4. Current limiting resistor

[Diagram of electronic circuit]
Basic + EMI + Short Circuit Protection + ESD
System considerations

- Wiring to the load introduces an inductance
  - Depending on the turn-off slew rate this can create a high voltage at the output
    - The ESD protection can be used to clamp the inductive energy
      - Energy capability changes with device size and dissipation time
      - Energy must be within SOA of the device
        - Base on T-SOA measurement data
        - Thermal simulation
    - If energy is too high for the power driver
      - An external clamp or freewheel diode must be added
Open Load (OL) and Short to GND (S2GND)

1. Reference voltage generation
2. Polarization buffer (current limited)
3. Open load comparator
4. Short to ground comparator
Open Load (OL) and Short to GND (S2GND) Simulation
Open Load (OL) and Short to GND (S2GND) Problems?

- There's a subtle error, a "snake in the grass"...
  - Out pin is high voltage and low voltage circuits require protection
Open Load (OL) and Short to GND (S2GND) Simulation

- Protection transistor introduces small voltage drop (20mV)
Questions?
‘Enabling The Smart Society’

Challenge:
“Ever increasing automotive requirements result in the demand to integrate complex MCU and Mixed Signal devices with features that are seemingly impossible to realize. What steps can be taken during development to achieve the unattainable?”

Solution:
“This class will introduce complexities dealt with during MCU and Mixed Signal development and the design steps taken to address some of these difficult automotive requirements.”
Please Provide Your Feedback...

- Please utilize the ‘Guidebook’ application to leave feedback

- Ask me for the paper feedback form for you to use...
Josh Lawton: Sr. Staff Engineer

Education
- BSEE: University of New Hampshire 1998

12 Years Semiconductor Industry Experience
- 11 Yrs: Elmos North America Inc.
  - Mixed signal design
    - Bar code scanner, squib drivers, buckle switch interface, sensor interface, door zone module, PWM relay driver, SWCAN, compass interface, EC mirror control, ion sense IGBT driver, and window lift
- 1 Yr: Renesas Electronics America Inc.
  - Mixed signal design
    - Airbag ASSPs