Course Introduction

- **Purpose**
  - This Part-A course discusses techniques that are used to reduce noise problems in the design of large scale integration (LSI) devices.

- **Objectives**
  - Understand the requirement for electromagnetic noise countermeasures.
  - Learn approaches and design methods for minimizing the electromagnetic interference (EMI) emitted by LSI devices.
  - Gain insight into how Renesas applies these techniques for handling noise problems in its microcomputer products.

- **Content**
  - 16 pages

- **Learning Time**
  - 20 minutes
Two types of noise:

- **Electromagnetic Compatibility (EMC) issues** encompass both types.

Noise reduction approaches:

- Techniques for reducing **EMI** (Electromagnetic Interference) — Cutting the noise emitted by a specific system, circuit or device that causes other devices/circuits to operate incorrectly.
- Techniques for decreasing **EMS** (Electromagnetic Susceptibility) — minimizing the effect that external noise has on the operation of a system, circuit or device.

Noise reduction: a goal common to both microcontroller (MCU) designers and the system engineers who apply those devices.

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Noise = “Unwanted electrical signals that produce undesirable effects in the circuits of control systems in which they occur.”

Noise Can Cause Big Problems
Why Is EMI Reduction Important?

Example of “real-world” effects: EMI can cause problems in the AV equipment and CIS products in an automobile.

- Noise is emitted by MCU and harness, causing EMI.
- Antenna picks up EMI noise, which degrades radio reception.

Battery
Audio-visual equipment, CIS products
Wiring harness (power line)
MCU
LSI device
Minimize ALL Sources of EMI

EMI reduction requires a comprehensive design approach and attention to detail

- No source of noise should be overlooked!

If measures are taken to deal only with secondary elements...

If measures are taken to deal only with elements of primary importance...

If measures are taken to deal with all important noise elements

EMI reduction requires a comprehensive design approach and attention to detail.

Minimize ALL Sources of EMI

EMI reduction requires a comprehensive design approach and attention to detail.
## Explanation of Terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
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<tbody>
<tr>
<td>Core</td>
<td>A microcontroller chip is composed of a core, I/O ports, and power supply circuitry. The core consists of the CPU, ROM, RAM, and blocks implementing timers, communication, and analog functions.</td>
</tr>
<tr>
<td>CPG</td>
<td>Clock Pulse Generator</td>
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<tr>
<td>Driver buffer</td>
<td>Output circuit transistors as well as output circuits for driving signals with large load capacitance and I/O port output transistors. Clock/bus driver, signals between blocks, etc.</td>
</tr>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference</td>
</tr>
<tr>
<td>EMS</td>
<td>Electromagnetic Susceptibility</td>
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<tr>
<td>Harness</td>
<td>Cables (wires) connecting a board and power supply or connecting one unit in a system to another.</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output Port</td>
</tr>
<tr>
<td>OSC</td>
<td>Oscillator</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Locked Loop</td>
</tr>
<tr>
<td>POR/LVD</td>
<td>Power-On Reset/Low-Voltage Detect functions</td>
</tr>
<tr>
<td>Power supply</td>
<td>Two power supplies are applied to the LSI: Vcc and Vss. The core power supply internal to the LSI is VCL (internal step-down). The Vss-based power supply routed through the LSI is VSL.</td>
</tr>
<tr>
<td>SSCG</td>
<td>Spread-Spectrum Clock Generator</td>
</tr>
<tr>
<td>WDT</td>
<td>Watchdog Timer</td>
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Pin Assignments Help Reduce EMI

- Microcontroller pin assignments should provide power supply and signal pin placements that closely match those of external LSI devices.
Arrangement of Key Pins

- Pins should be arranged in an electrical potential gradient
- Pin layout should concentrate key pins in one area
- Arrangement should make it easy to mount bypass capacitors for noise countermeasures
- Standardized layouts promote design consistency

Key pins are concentrated in a single location

Effects of electrical potential differences are minimized

Pin arrangement makes it easy to mount bypass capacitors between power supply lines and ground lines.

Capacitor for Reset

Oscillation capacitors

Oscillation capacitors

Ceramic bypass capacitor

Tantalum bypass capacitor
Power Supply Pin Assignments

- Placing power supply pins in pairs near each other makes it easy to mount bypass capacitors where they can be effective.

**Diagram:**
- CORE-1 power supply pin
- CORE-2 power supply pin
- I/O PORT-1 power supply pin
- I/O PORT-2 power supply pin

**Capacitors:**
- \( C_1, C_2, C_3, C_4 \) = Power supply bypass capacitors
- \( C_A, C_B \) = Step-down power supply (Vdd) stabilization capacitors

**Ports and Voltages:**
- Vcc
e- Vss
- Vcl (Vdd)
- Vcce
- Vsse
- Vsscore
- I/O PORTR1
- I/O PORTR2
Analog vs. Digital Signal Pins

- For best analog circuit performance, some types of digital signal pins must not be located close to the analog signal pins.

- The following types of digital signal pins should not be placed in these locations:
  - High-current ports
  - Clock-related ports
  - High-speed telecom ports
Power Supply Circuit

- Internal step-down power supply circuit runs off 5V, produces precise lower voltage (Vdd) for core

  - The lower the core voltage, the greater the EMI reduction
  - A slower slew rate cuts EMI

<table>
<thead>
<tr>
<th>Step-down voltage</th>
<th>None</th>
<th>Low</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMI</td>
<td>High</td>
<td>Reduced</td>
</tr>
</tbody>
</table>

Vcc = 5.0V
Vdd (core voltage) = 1.2V

A low Vdd reduces power consumption, too.

A/D, D/A

Core:
- CPU
- ROM
- RAM
- TIMERS
- SCI
- Etc.

External step-down power supply circuit stabilization capacitor

5V I/O

Step-down circuit

Layout of internal step-down circuit (conceptual)
Step-down Power Supply Voltage

- Step-down voltage is used at the 0.5µm process generation and below to reduce EMI.
- Process limitations at 0.35µm and 0.5µm process generations and below mandate lower core voltages.
- Further decreases in Vdd are expected, allowing additional EMI reductions and power savings.
EMI Filter in Step-down Supply

- **π**-type R-C filter is located between step-down circuit and core
  - Uses parasitic capacitances of step-down transistors and core and parasitic resistance of internal power supply lines

![EMI Filter Diagram](image-url)
Wiring for Power Supply Lines

- In devices with multiple power supply pins, Vcc and Vss should be...
  - Supplied in pairs
  - Located near each other
- This design approach ensures that the chip’s internal power supply lines do not cross
Main Power Supply Lines in Core

- Power supply lines to I/O and core are separated
- Mesh configuration is used for supply lines to core
Capacitors in Power Supply Lines

- Capacitors can be placed in various locations within the LSI device
- They deliver supplemental charge needed for driving digital-circuit switching
  - Without embedded capacitors, ripple component of power supply waveform is large
  - With capacitors, ripple component is small and EMI is reduced
Course Summary

- Types of noise (EMI and EMS) in microcomputers
- Importance of EMC
- Reducing EMI by using optimum methods for pin assignments, step-down power supply design, and on-chip power wiring

For more information on specific devices and related support products and material, please visit our Web site: http://america.renesas.com