Agenda

This module contains a description of specific features of the RX 10 Bit ADC “ADa”.

For basic ADC technology and terms refer to ADC Technology Module and ADC Operating Mode Modules

For overview of ADC features for a specific group refer to RX Family Overview Module. The Overview module describes number of channels, conversion times and other specific items

Contained in this Module
- Block Diagram
- Operating Modes
- Data Register
- Self – Diagnostic Feature
- Sampling Time Adjustment
- Usage Notes
This figure shows a typical block diagram of the 10 Bit A-D converter in the RX MCU. The multiplexed data inputs AN0 to AN7 are highlighted by the red box. ANEX0 and ANEX1 are the extended input which is described later and are not included in the RX62N group.

AVcc and AVss are the analog inputs that power the block while Vrefh and Vrefl are the reference inputs which drive the 10 bit D/A used in the successive approximation process.

On the right side of the block diagram the internal data bus connection is shown along with the interrupt signal.

The RX ADC allows an asynch trigger using the ADTRG pin and also provides a synchronized trigger. The module can also be triggered by software or synchronously from various timer signals including compare match and input capture functions. Refer to the HW manual for the specific device to verify which timer signals can be used.

The RX ADC has various clocks which can be selected as the source for the AD clock, in the diagram it can be seen that PCLK or PCLK divided by 2, 4 or 8 can be selected. Reference the HW manual for the specific device to determine which clock sources can be selected and for details on setting up the clock dividers.

The block diagram also shows the individual conversion result registers (ADDRA – ADDRH) and the various control and mode registers.

For more detail on basic SAR operation please refer to the ADC Technology and the ADC Operating Mode Modules.
There are different operating modes of the ADC that can be selected.

Single Mode performs only one conversion on only one analog input pin. If interrupts are used the interrupt is triggered after the single conversion is done.

The second mode is called Continuous Scan Mode. In this mode the user is able to select one analog input pin, or a range of pins. The ADC will then perform conversions on those pins sequentially. When all of the selected analog input pins have been converted, the ADC will start back at the first pin again. This process is continued until the ADC is told to stop. If interrupts are enabled for the ADC an interrupt is generated every time the conversion for the last input pin has finished.

The last mode is One-Cycle Scan Mode. This mode is similar to Continuous Scan Mode except that the analog input pins are only looped through once. Once the selected pins have been converted once, the ADC stops. If the ADC interrupts are enabled then an interrupt will fire at this time.
The ADC Data registers store the results of the ADC conversion. Each channel has its own result register. The 10 bit data can be right aligned (click and pause) or left aligned (click and pause) depending on settings in the control registers. Unused or padded bits in the result are always zero so there is no need to mask the extra bits. The reset value of the registers is zero.
One of the unique features of the RX ADC peripheral is the inclusion of a self-diagnostic feature which simplifies verification of the operation of the ADC system. When enabled the diagnostic feature allows converting internally derived 0V, ½ Vref or Vref. The value can then be read from the results register and can be used to compare to external system signals which are converted.

The typical way this is used is as follows. First, set the ADC unit to be in Single Mode. Then select that only analog input channel AN0 is selected. With these settings trigger the A/D conversion using the software trigger. When the conversion is finished it can be read from the AD data register A and the result verified.
A complete AD conversion consists of three components:

An A/D conversion start delay time represented by $t_D$

A sampling time which is the time where the sample and hold capacitor is charged. This is shown as $t_{SPL}$ in the diagram.

The actual successive approximation time which is represented by $t_{SAM}$, is fixed at 25 clock cycles.

When using repeat mode the start delay only occurs for the first conversion in the sweep. The following channel conversion times are equal to the sample time plus the conversion time.

In the “Fundamentals of ADC” module one of the sources of error that was described was due to a high source impedance which did not allow the sample capacitor to charge sufficiently. The RX ADC has the ability to modify the length of time that the sample capacitor is connected to the input, allowing the capacitor to fully charge even with higher source impedances.
The ADDSTR register is an 8 bit register which is used to modify the sampling time of the ADC system. The adjustment can be used to lengthen the sample time when the source impedance is high or the number of sample clocks can be reduced if the peripheral clock (PCLK) is slow.

The formula for calculating the resulting sampling time is to divide the value in the ADDSTR register by the frequency of the ADCLK.

The address and value for the ADDSTR register after reset are shown for the RX62N Group. Check the hardware manual for the minimum allowable setting, for the RX62N the minimum setting is 02h.
The table shown above is provided in the HW manual. It summarizes the various times required to complete an ADC conversion. Notice that the A/D conversion delay is not included except in single mode and the first conversion of a scan.
This feature is not supplied the RX62 group. Please check the device HW manual to see if this feature is supported for the specific device you are interested in.

Typically if an external OpAmp is used to scale the ADC inputs an external analog mux is also required to select the various inputs to be applied to the OpAmp input. The RX ADC block allows connecting to an external OpAmp after the input analog mux so the need for an external mux is eliminated. The multiplexed analog input is output on the ANEX0 output. This signal is processed by the external OpAmp or other circuitry then input to the conversion circuit in the MCU using the ANEX1 pin.

Once the appropriate control register are configured scanning inputs and reading conversion results are the same as when the external circuit configuration is not used. The conversion time is increased by the latency of the external circuits that are used.
The ADC block provides a conversion complete interrupt for each ADC unit. The interrupt occurs once a one-shot mode conversion is complete or after all channels are converted when using a scan mode conversion. The interrupt signal can be used for standard interrupt operation or can be used as an activation signal for DTC (Data Transfer Controller) or DMAC (Direct Memory Access Controller) operation. Refer to the DTC/DMAC modules for more details on the operation and use of those modules.

When entering power down states the ADC module will consume the same current as it would when converting in an active mode. Therefore the ADC should be disabled by selecting SW trigger and setting the ADST bit to 0 before entering the power down state.
In this module we looked at the basic operation of the RX 10 Bit ADC, including describing the basic block diagram operation and single mode and continuous scan modes of operation. The data registers and data alignment capabilities were also described.

The RX 10 bit ADC block self-diagnostic features were highlighted along with the capability to adjust the ADC sampling time which can be useful when source impedance is high or a very slow PCLK is being used.

Finally the ability to generate interrupts or trigger DMAC or DTC transfers was described along with the precaution to disable the ADC prior to entering low power mode.

You may want to refer to the RX Technical Marketing Overview Module for more information regarding a specific RX group or the ADC Technology Module and ADC Operating Mode Modules for more general information regarding ADCs in MCU systems.