Course Introduction

- **Purpose:**
  - This course provides an overview of the Renesas SuperH™ series of 32-bit RISC processors, especially the microcontrollers in the SH-2 and SH-2A series

- **Objectives:**
  - Learn the design concepts behind the SuperH™ series architecture
  - Understand the key features and functions of microcontrollers in the SH-2 and SH-2A series
  - Discover the advantages of devices in the series for a wide range of embedded system applications

- **Content:**
  - 19 pages
  - 3 questions

- **Learning Time:**
  - 20 minutes
SuperH™ Series Basics

- Popular microcontrollers and microprocessors based on the well-established and expanding SuperH™ 32-bit RISC engine architecture

- Architecture design concepts:
  - High performance
  - Upward compatibility
  - High code density
  - Low power consumption
  - Innovative technology

- Highlights of SuperH™ devices:
  - Multiple product lines with different SuperH™ CPU cores
  - High integration with advanced on-chip peripheral functions
  - On-chip flash memory
  - Outstanding features for the price
  - Solid technology roadmap

- Applications:
  - Automotive systems, consumer electronics, communication equipment, industrial control systems, office automation products, among many others
SuperH™ Series CPU Cores

- The choice of an architecture is one of the most important design decisions in the development of an embedded system.
  - SuperH™ cores are available in many different optimized versions.

For high-performance applications and open-OS support:

- SH-4A (266 to 600MHz, Superscalar CPU, FPU)
- SH-4A (266 to 600MHz, Dual Core)
- SH-2A (100 to 200MHz, Superscalar CPU, FPU, Dual Core)

For real-time control applications:

- SH-1 (Up to 20MHz, 32-bit multiplier)
- SH-2 (Up to 200MHz, MMU, Cache)
- SH-3 (Up to 200MHz, Superscalar CPU, FPU)

**Maximum performance (please check latest data):**

- SH-1: 10 DMIPS (20MHz)
- SH-2: 104 DMIPS (80MHz)
- SH-2A: 480 DMIPS (200MHz)
- SH-3: 260 DMIPS (200MHz)
- SH-4: 430 DMIPS (240MHz)
- SH-4A: 1040 DMIPS (600MHz)
Compatibility, Code Density

- **Upward software compatibility:**
  - Same basic CPU core underlies versions with enhanced instruction sets
  - Extensive processor choices span diverse feature sets and many levels of performance
  - Software reuse makes possible a faster time to market for new designs and upgrades

- **High code density:**
  - 16-bit instruction length typically enables 33% greater code density
  - 16-bit instructions provide double the bus bandwidth; increase cache efficiency; and decrease the need for external memory
Low Power, Innovative Technology

- **Low power consumption:**
  - Design goal is to balance power with performance to achieve excellent MIPS/W ratios
  - Power-saving circuit designs and power-down operating modes boost power efficiency
  - Devices are built with low-power sub-micron CMOS processes

- **Innovative technology:**
  - Advanced design, processing and packaging techniques
  - On-chip flash, peripherals and IP boost functionality, performance and value
  - World-class hardware/software tools make system development easier and more effective
Which statements about the SuperH architecture design are correct? Select all that apply and then click Submit.

- The SuperH family offers code compatibility so that software can be reused across a range of applications.
- Innovative technology such as the integration of complex peripherals enables SuperH products to deliver solutions for many applications.
- Like traditional 32-bit RISC architectures, the devices in the SuperH series only use a full 32-bit Opcode instruction length.
- A 16-bit instruction length doubles bus bandwidth, boosts cache efficiency, and reduces the need for external memory.
Enhanced Features of SH-2A CPU

- Operates at higher frequencies
  - Up to 200MHz now, 300MHz planned
- Is a superscalar design
  - Executes two instructions/cycle for very high throughput
- Uses register banks for fast interrupt response, decreased latency
- Adds instructions that reduce program size and increase efficiency
- Has built-in hardware multiplier-accumulate unit (MAC) for DSP-type operations
Performance Comparison

- **Execution performance**
  - SH-2A at 160MHz is 4.8x faster than SH-2 at 50MHz
  - SH-2A at 200MHz is 6x faster than SH-2 at 50MHz

- **Interrupt switching time**
  - SH-2A processes interrupts in 6 cycles
  - SH-2 processes interrupts in 37 cycles
  - SH-2A switching time at 200MHz is 1/25 that of SH-2 at 50MHz

- **Program code size**
  - SH-2A code is 25% more compact than SH-2 code
Is the following statement about the SH-2A core true or false? Click Submit when you are finished.

“Instruction execution is enhanced by the implementation of a superscalar architecture.”

- True
- False
# MPU/MCU Product Roadmap / Microprocessors

## Highest Performance General Purpose

<table>
<thead>
<tr>
<th>Series</th>
<th>Model</th>
<th>Clock Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>SH3-DSP</td>
<td>SH775x</td>
<td>240MHz</td>
</tr>
<tr>
<td>SH4</td>
<td>SH7780</td>
<td>400MHz</td>
</tr>
<tr>
<td>SH4A</td>
<td>SH7785</td>
<td>600MHz</td>
</tr>
<tr>
<td>SH-4 Dual Core</td>
<td>SH7786*</td>
<td>Dual Core 2x SH 4A 533MHz</td>
</tr>
</tbody>
</table>

* under development

## Industrial/Ethernet Connectivity

<table>
<thead>
<tr>
<th>Series</th>
<th>Model</th>
<th>Clock Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>SH3-DSP</td>
<td>SH7710/12/13</td>
<td>200MHz</td>
</tr>
<tr>
<td>SH4</td>
<td>SH7760</td>
<td>200MHz</td>
</tr>
<tr>
<td>SH4A</td>
<td>SH7763</td>
<td>266MHz</td>
</tr>
<tr>
<td>SH4A</td>
<td>SH7764</td>
<td>324MHz</td>
</tr>
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</table>

## Low Power Multimedia

<table>
<thead>
<tr>
<th>Series</th>
<th>Model</th>
<th>Clock Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>SH3-DSP</td>
<td>SH7727</td>
<td>160MHz</td>
</tr>
<tr>
<td>SH3-DSP</td>
<td>SH7720/21</td>
<td>133MHz</td>
</tr>
<tr>
<td>SH4A-DSP</td>
<td>SH7722</td>
<td>266MHz</td>
</tr>
<tr>
<td>SH4A-FPU</td>
<td>SH7723</td>
<td>400MHz</td>
</tr>
<tr>
<td>SH4A-FPU</td>
<td>SH7724*</td>
<td>500MHz</td>
</tr>
</tbody>
</table>
MPU/MCU Product Roadmap / Microcontrollers

- SH-2A SH7206 200MHz
- SH-2A SH7201 120MHz
- SH-2A SH7203 200MHz
- SH-2A SH7211 160MHz
- SH-2A SH728/6F 100MHz
- SH-2 SH7147 SH7142 80MHz
- SH-2 SH7146 SH7149 80MHz
- SH-Tiny SH7125 SH7124 50MHz
- SH-2A Dual Core SH7205 2 x 200MHz
- SH-2A SH767x 200MHz
- SH-2A* SH7216F 200MHz

- Romless
- High End
- Mid Range
- Tiny

* Production in Q2/10
SuperH™ 32-bit Microcontroller Lineup

- Optimized for implementing single-chip or minimum-chip embedded systems:
  - Providing performance, power consumption and peripheral functions matched to the needs of important markets:
    - Consumer
    - PC/AV
    - Automotive
    - Industrial
    - Many others

- **SH-2**
  - **SH761x**
    - 176pin
    - 100/125MHz
    - 18 / 19
    - Integrate PHY option
    - Ethernet ROM-less

- **SH-2A**
  - **SH76xx**
    - 256pin
    - 200MHz
    - 05 / 06 / 03 / 01
    - USB + SD interface
    - Ethernet ROM-less

  - **SH720x**
    - 240/176pin
    - 120MHz
    - 85 / 86 / 11 / 16
    - LCD Driver option
    - ROM-less

  - **SH722x**
    - 176/144pin
    - 100-200MHz
    - 85 / 86 / 11 / 16
    - 512k – 1M
    - High End Flash

  - **SH724x**
    - 100pin
    - 100MHz
    - 43
    - 256k
    - Mid End Flash

- **SH71xx**
  - 80/100pin
  - 80MHz
  - 37 / 36 / 47 / 42 / 46 / 49
  - 256k – 512k
  - Mid End Flash

- **SH71xx**
  - 48-64pin
  - 50MHz
  - 25 / 24
  - 32k – 128k
  - SH/Tiny
SH767x

- **SH2A CPU Core**
  - 200MHz = 480DMIPS
  - Superscalar architecture
  - 2 instructions executed per clock tick
  - Integrated FPU

- **On Chip Memory**
  - 32kbytes on chip RAM
  - 16kbytes Cache
  - HIF: 4K dual ported RAM accessible from external host & CPU
  - BSC for external Memory 100MHz 32bit
  - SD Card interface

- **Connectivity**
  - Ethernet MAC 10/100, MII, 512Byte FiFO, EDMA
  - USB 2.0 high speed host or function
  - 1ch IIC
  - 3ch SCIF

- **Timers**
  - CMT – 2ch 16-Bit timer
  - Watchdog Timer

- **Other**
  - 8ch DMA
  - SD Card interface option
  - Encryption Module
  - Serial Sound Interface (SSI)

- **Debug**
  - UBC With 2 break channels
  - H-UDI for JTAG + Boundary scan

- **Digital I/O**
  - 86 I/O pins (+ 8 input only)

- **Power Supply Voltage**
  - 3.3V +/- 0.2V for I/O
  - 1.2V +/- 0.1V for internal

- **Packages**
  - FBGA-256 (17 x 17 mm², 0.8 mm pitch)

- **Temperature Ranges**
  - -20 -> +70 °C
  - -40 -> +85 °C

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SH7205

- **2x SH2A CPU Core**
  - 2 x 200MHz = 960DMIPS
  - 2 x 2 instructions executed per clock tick
  - 2 x Integrated FPU

- **On Chip Memory**
  - 96kbytes on chip RAM
  - 16kbytes low-power RAM
  - 2 x 16kbytes Cache
  - BSC for external Memory 66MHz 32-Bit

- **Analogue**
  - ADC: 8ch 10-Bit (3.9µs Conversion time)
  - DAC: 2ch 8-Bit

- **Connectivity**
  - USB 2.0 high speed host or function
  - 2ch CAN
  - 2ch SSU
  - 6ch SCIF
  - 4ch I2C

- **Timers**
  - MTU2 – 5ch 16-Bit timer for Motor Control
  - CMT – 4ch 16-Bit timer
  - Watchdog Timer

- **Other**
  - 14ch DMA
  - 2D engine for (480 × 234) or (320 × 240) + RGB-out

- **Debug**
  - UBC with 2 break channels
  - H-UDI for JTAG

- **Digital I/O**
  - 96 I/O pins (+ 11 input only)

- **Power Supply Voltage**
  - 3.3V +/- 0.3V for I/O
  - 1.2V +/- 0.1V for internal

- **Packages**
  - BGA-272 (17 x 17 mm2, 0.8 mm pitch)

- **Temperature Ranges**
  - -20 -> +85 °C
SH7203

- **SH2A CPU Core**
  - 200MHz = 480DMIPS
  - 2 instructions executed per clock tick
  - Integrated FPU

- **On Chip Memory**
  - 64kbytes on chip RAM
  - 16kbytes low-power RAM
  - 16kbytes Cache
  - BSC for external Memory 66MHz 32-Bit

- **Analogue**
  - ADC: 8ch 10-Bit (3.9us Conversion time)
  - DAC: 2ch 8-Bit

- **Connectivity**
  - USB 2.0 high speed host or function
  - 2ch CAN
  - 2ch SSU
  - 4ch SCIF
  - 4ch IIC

- **Timers**
  - MTU2 – 5ch 16-Bit timer for Motor Control
  - CMT – 2ch 16-Bit timer
  - Watchdog Timer

- **Other**
  - 8ch DMA
  - SD Card interface option (on 7263)

- **Debug**
  - UBC With 2 break channels
  - H-UDI for JTAG
  - Advanced User Debug

- **Digital I/O**
  - 82 I/O pins (+ 16 input only + 1 output only pin)

- **Power Supply Voltage**
  - 3.3V +/- 0.3V for I/O
  - 1.2V +/- 0.1V for internal

- **Packages**
  - LQFP-240 (32 x 32 mm², 0.5 mm pitch)
  - BGA-272 (17 x 17 mm², 0.8 mm pitch)

- **Temperature Ranges**
  - -20 -> +85 °C
SH7216 Series

- **SH2A CPU core**
  - SH-2A (SuperH RISC Engine) Single core
  - FPU (single precision, double precision)
  - 32-bit multiplier (32-bit x 32-bit -> 64-bit)
  - Harvard architecture

- **Operating frequency**
  - CPU: bus/peripheral: 100/200MHz: 50MHz/50MHz

- **Power supply voltage**
  - 3.3V+-0.3V(core,I/O), 5.0V+-0.5V(A/D)

- **On-chip memory**
  - 512KB/768KB/1MB Flash memory
  - 64KB/96KB/128KB RAM (64KB:1 cycle access)
  - 32k Data Flash (R/W 30K :Target) with BGO function

- **External memory interface**
  - SDRAM, Byte-selection SRAM, burst ROM
  - 8-bit, 16-bit and 32-bit

- **Peripheral functions**
  - Multifunction 16-bit PWM timer: 6ch(MTU2), 3ch(MTU2S)
  - Port output enable (POE)
  - 16-bit cycle timer: 2ch
  - Watchdog timer: 1ch
  - I2C bus interface: 1ch
  - USB2.0 function (full speed): 1ch
  - DMA controller: 8ch + DTC
  - 12-bit A/D converter: 4ch x 2 Units
    (1ch supports 3ch simultaneous S/H)
  - SCI: 4ch
  - SCIF: 1ch (16-stage transmit and receive FIFO)
  - JTAG interface
  - RSPI I/F
  - RCAN I/F
  - Ether Net MAC I/F

- **Packages**
  - LQFP176pin (20mm x 20mm 0.4mm pitch)
  - LQFP176pin (24mm x 24mm 0.5mm pitch)
  - BGA176pin (13mm x 13mm 0.8mm pitch)
SH7285 / 7286

- **SH2A CPU Core**
  100MHz = 240DMIPS
  2 instructions executed per clock tick

- **On Chip Memory**
  1M-512kB MONOS Flash
  32-24kB on chip RAM
  BSC for external Memory 50MHz 32-Bit

- **Analogue**
  ADC: 8-12ch 12-Bit (1.0us Conversion time)
  DAC: 0-2ch 8-Bit

- **Connectivity**
  USB 2.0 full speed function
  0-1ch CAN
  1ch SSU
  5ch SCI(F)
  1ch IIC

- **Timers**
  MTU2 – 6ch 16-Bit timer for Motor Control
  MTU2S – 3ch 16-Bit timer for Motor Control
  CMT – 2ch 16-Bit timer
  Watchdog Timer

- **Other**
  8ch DMA
  Data Transfer Controller (DTC)

- **Debug**
  UBC with 2 break channels
  H-UDI for JTAG
  Advanced User Debug

- **Digital I/O**
  91-101 I/O pins (+ 8-12 input only)

- **Power Supply Voltage**
  5.0V +/- 0.5V for Analogue
  5.0V +/- 0.5V OR 3.3V +/- 0.3V for I/O

- **Packages**
  LQFP-176 (20 x 20 mm², 0.4 mm pitch)
  LQFP-176 (24 x 24 mm², 0.5 mm pitch)
  LQFP-144 (20 x 20 mm², 0.5 mm pitch)

- **Temperature Ranges**
  -20 -> +85 ° C
  -40 -> +85 ° C

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SH7285, SH7286 block diagram
SH7137 / SH7136

- **SH2A CPU Core**
  - 80MHz
  - 32 x 32 MAC Unit

- **On Chip Memory**
  - 256kB MONOS Flash
  - 16kB on chip RAM
  - BSC for external Memory 40MHz 8-Bit

- **Analogue**
  - ADC: 12 - 16ch 12-Bit
  - 1.25us Conversion time.

- **Connectivity**
  - 3ch SCI(F)
  - 1ch SSU
  - 1ch IIC
  - 1ch CAN

- **Timers**
  - MTU2 – 6ch 16-Bit timer for Motor Control
  - MTU2S – 3ch 16-Bit timer for Motor Control
  - CMT – 2ch 16-Bit timer
  - Watchdog Timer

- **Other**
  - Data Transfer Controller (DTC)

- **Debug**
  - UBC with 2 break channels
  - H-UDI for JTAG

- **Digital I/O**
  - 57-44 I/O pins (+ 16-12 input only)

- **Power Supply Voltage**
  - 5.0V +/- 0.5V for Analogue
  - 5.0V +/- 0.5V OR 3.3V +/- 0.3V for I/O

- **Packages**
  - LQFP-100 (14 x 14 mm², 0.5 mm pitch) (SH7137)
  - LQFP-80  (14 x 14 mm², 0.65 mm pitch) (SH7136)

- **Temperature Ranges**
  - -20 -> +85 °C
  - -40 -> +85 °C
SH7125 / SH7124

- **SH2 CPU Core**
  50MHz
  32 x 32 MAC Unit

- **On Chip Memory**
  16-128kB MONOS Flash
  4-8kB on chip RAM

- **Analogue**
  ADC: 2 x 4ch 10-Bit
  2.0us Conversion time

- **Connectivity**
  3ch SCI(F)

- **Timers**
  MTU2 – 6ch 16-Bit timer for Motor Control
  CMT – 2ch 16-Bit timer
  Watchdog Timer

- **Debug**
  UBC with 2 break channels
  H-UDI for JTAG

- **Digital I/O**
  37-23 I/O pins (+8 input only)

- **Power Supply Voltage**
  5.0V +/- 0.5V

- **Packages**
  QFP-64 (14 x 14 mm², 0.8 mm pitch) (SH7125)
  LQFP-64 (10 x 10 mm², 0.5 mm pitch) (SH7125)
  LQFP-48 (10 x 10 mm², 0.65 mm pitch) (SH7124)
  VQFN-64 (8 x 8 mm², 0.4 mm pitch) (SH7125)
  VQFN-52 (7 x 7 mm², 0.4 mm pitch) (SH7124)

- **Temperature Ranges**
  -20 -> +85 °C
  -40 -> +85 °C
Match each SuperH microcontroller term to its description by dragging the letters on the left to their appropriate locations on the right. Click Submit when you are finished.

SH-2A
Big solutions in small packages for designs that have moderate peripheral and memory requirements

SH/Tiny
Microcontroller family that provide functions for Ethernet connectivity as well as system control tasks

H-UDI
Popular Superscalar 32-bit RISC CPU core that operates at clock speeds up to 200MHz

SH767x
On-chip debugging interface that enables low-cost debugging tools
Course Summary

- SuperH™ family of microcontrollers and microprocessors
- SH-2 microcontroller core and devices
- SH-2A microcontroller core and devices