ID 311C: Utilizing JTAG / boundary scan and JTAG emulation for board and system level test and design verification

GOEPEL Electronics
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12 October 2010
Version 1.3
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- Managing Director of North American Operations at GOEPEL Electronics LLC at Austin, TX
  - responsible for GOEPEL's operations in the USA, Canada, and Mexico
  - providing support and consulting services to North American clients
  - GOEPEL was founded in 1991 and has ~160 employees worldwide, active in JTAG/boundary scan, AOI, AXI, and Functional Test

- Prior Experience:
  - Field Application Engineer for JTAG/boundary scan supporting GOEPEL customers in Germany and then Europe
  - BSEE from the University of Applied Sciences at Mittweida, Germany
In the session 110C, Renesas Next Generation Microcontroller and Microprocessor Technology Roadmap, Ritesh Tyagi introduces this high level image of where the Renesas Products fit. The big picture.
This is where our session, ‘ID 321C - Utilizing JTAG / boundary scan and JTAG emulation for board and system level test and design verification’ is focused within the ‘Big picture of Renesas Products’
Here are the MCU and MPU Product Lines, I am not going to cover any specific information on these families, but rather I want to show you where this session is focused.
These are the products where this presentation applies
### Innovation

<table>
<thead>
<tr>
<th>Design verification and prototyping</th>
<th>Manufacturing test and debug</th>
<th>End of line (system) test</th>
<th>Field service / warranty/repair</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>On-Chip / In-Circuit Emulation</strong></td>
<td><strong>IEEE 1149.x</strong></td>
<td><strong>IEEE 1149.x</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>JTAG / boundary scan</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Functional test</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>IEEE 1149.x (JTAG / boundary scan)</strong> + <strong>On-Chip Emulation</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Functional test</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Intelligent boundary scan solutions

GOEPEL is a technology leader in JTAG / boundary scan – creating new, innovative ways to extend the reach of boundary scan beyond pure structural test applications.
**Agenda**

- Benefits and limitations of IEEE Std. 1149.1 for board level debug and test
- Overview of board and system level JTAG/boundary scan applications
- Utilization of On-Chip Emulation resources for board level connectivity test applications
- Interlaced JTAG Emulation and boundary scan testing
- Summary of fault coverage improvements and other benefits

- Benefits and limitations of IEEE Std. 1149.1 for board level debug and test
- Overview of board and system level JTAG/boundary scan applications
- Connectivity Test
- Device Programming / Configuration
- On-Chip Emulation
- Integration and collaboration with other (non-JTAG) test equipment (such as In-Circuit Test, Flying Probe Test, Functional Test, etc.)
- Fault Insertion, Debug, Troubleshooting
- Concept of utilization of On-Chip Emulation resources for board level connectivity test applications
- Interlaced JTAG Emulation and boundary scan testing
- Summary of fault coverage improvements and other benefits when utilizing On-Chip Emulation resources and boundary scan for board level test
Key Takeaways

By the end of this session you will be able to:

- Identify potential board and system level test applications supported by JTAG/boundary scan on specific board/system designs;

- Discuss potential test strategies involving JTAG/boundary scan with test engineering / production test groups
JTAG / boundary scan in a nutshell
• IEEE 1149.1 compliant devices provide various testability features:
  • TAP (TCK, TMS, TDI, TDO, optional /TRST)
  • TAP Controller (16-state finite state machine)
  • Boundary register (comprised of boundary scan cells, providing I/O pin control in boundary scan [Extest] test mode)
  • Bypass register
  • Instruction register
  • ID Register (optional)
  • other optional resources may be implemented
  • interconnect test based on using Extest capability in IEEE 1149.1 compliant devices to test for manufacturing defects (opens, shorts, stuck-at’s) on I/O pins
  • test of connections to non-boundary scan devices based on stimulation and observation of cluster functions (e.g. writing to / reading from memory devices, evaluating logic functions, etc.)
  • boundary scan (IEEE 1149.1 compliant) devices are controlled through a JTAG scan chain, providing access to their TAPs
If you have experience with boundary scan, you most likely are familiar with the limitations JTAG/boundary scan has. By the way, if you are not familiar with the boundary scan technology, we offer seminars, webinar sessions, and learning material that can help you get up to speed. So, despite all the benefits boundary scan provides, there are some shortcomings. In particular, IEEE 1149.1, the core specification for boundary scan technology, is restricted to digital circuitry. There is, of course the IEEE 1149.4 specification, which defines boundary scan resources for analog and mixed signal devices, however, there is a very limited number of off-the-shelf components available that support this technology.

Another shortcoming of boundary scan is rooted in the basic concept of converting serial test vectors into parallel test pattern applied to I/O pins on a device. This serial-to-parallel conversion, combined the fact that the test vectors are shifted at a relative low speed of several Megahertz, results is a pretty slow toggle rate on device I/O pins. This toggle rate is typically in the range of a few KiloHertz, which is why we consider boundary scan connectivity tests as quasi-static tests. A sequence of parallel test pattern cannot be applied fast enough on the device I/O pins to do any true dynamic testing. (Contrast this with DDR memory interfaces, for example, which operate at dozens or hundreds of Megahertz.) One way of compensating for this limitation of boundary scan technology is the execution of Built-In Self Tests which, if existent in a particular JTAG/boundary scan device, can be controlled through the JTAG port of that component.

Test access to circuitry on the Unit Under Test, of course, is determined by the extend boundary scan resources available in devices on that UUT. We can compare boundary scan cells embedded in devices to test points accessible with a nail probe on an In-Circuit Tester. If a certain net or circuit node doesn't have an accessible test point, the ICT cannot directly include this net in any tests. Similarly, if there is not boundary scan cell connected to a certain net, then this net cannot be directly controlled or observed in any boundary scan tests. A number of such nets may be testable as part of Cluster Tests (where such nets are indirectly connected to boundary scan I/O's), but the diagnostic detail is often reduced in such cases.

So, with these shortcomings in mind, here are some suggestions on how the boundary scan test coverage can be improved:
- Test points or connector pins could be accessed with tester I/O signals in order to include circuit parts that may otherwise not be fully testable with just the boundary scan resources embedded in the devices on the UUT;
When we compare boundary scan and device emulation, we can identify benefits and limitations for both.

Boundary scan is great for structural test, the detection and diagnosis of open pins and shorted nets, for example. Boundary scan tests are generated automatically, with a predictive test coverage, and provide pin level diagnostics. Furthermore, boundary scan can be used for system level test and for In-System Programming. On the downside, boundary scan is inefficient for Flash programming and has limitations when it comes to testing dynamic parameters of the UUT. Complex non-boundary scan clusters limit the diagnostic resolution or even make boundary scan tests impractical. And not to forget, the device must feature a boundary scan Register in order to provide access to its I/O pins. Some lower-cost microcontrollers, for example, implement a JTAG port for device emulation, but no boundary scan Register, therefore not supporting boundary scan tests.

Emulation, on the other hand, is a great way to support functional tests. It can be used to extend the fault coverage to include dynamic faults, for example. Since Emulation runs at-speed, typically utilizing system clocks, Flash programming can be quite a bit faster with Emulation than with boundary scan. On the downside, On-Chip Emulation typically requires microcontroller specific hardware - or JTAG PODs. Since there is no or very limited ATPG tools and no predictive test coverage for emulation tests, test development takes more time and the quality of diagnostics is typically lower than with boundary scan. Common emulation tools may also be limited in their capabilities to support system level test and in-system programming.

So, how can we get the best of both worlds?
Boundary scan test and Emulation test are complementary technologies, and system solutions supporting synergies between the two can combine the benefits of boundary scan with the benefits of device emulation and can overcome the major limitations of both methods.

GOEPEL provides a technology called VarioTAP that utilizes on-chip programming and access to on-chip emulation functions for board level connectivity tests and mini-functional tests.
Classification of boundary scan applications

One of the most common types of boundary scan application is board level connectivity test. This class of applications includes different types of tests that focus on manufacturing defects such as open pins and shorted nets. This covers mostly the digital parts of the circuitry.

The next class of boundary scan applications focuses on in-circuit- or in-system programming of CPLD, FPGA, serial EEPROM and Flash devices, as well as on-chip memory in micro controllers or digital signal processors, for example.

The third class of applications utilizing the Test Access Port defined in IEEE 1149.1 focuses on device emulation functions applied to board level tests. This includes the functional verification of bus interfaces integrated in the boundary scan device as well as structural and functional verification of board level connections to memory devices and bus interface controllers.

The last class of boundary scan applications involves additional tester hardware in order to improve the test coverage by including peripheral interfaces or by providing extra test access beyond the boundary scan cells built-in to devices on the Unit Under Test.
Utilization of On-Chip Emulation resources for board level connectivity test applications

Now let's take a quick look at a typical stand-alone boundary scan tester setup ...
Emulation Test

Generic µP / MCU / CPU model (On-Chip Resources)

- Bus IF Type A
- Bus IF Type X
- Internal Circuits
- System Bus IF
- Core
- Flash
- Analog I/O
- Digital I/O
- Mixed I/O
- On-Board Resources: DRAM, External Periphery, Bridges, etc.

Application Type A: Programming Functions for On-Chip or external Flash
Application Type B: Bus Control Functions for Bus Emulation Test
Application Type C: Test Functions for On-Chip Resources

- Higher fault coverage than pure boundary scan
- Single source, one S/W & H/W environment
- Seamlessly integrated (SYSTEM CASCON + SCANFLEX)
- Multi-Family PODs (supporting various processor types and families)
- Up to 8 TAP, flexible TAP parameter programming
- High-speed TCK support (80MHz)
- Ultra-fast FLASH programming support
- Unique concept of language based debug, emulation, and test via JTAG and potentially other interface ports

If we look at a generic micro-controller, such a device typically has a core that is accessible from the JTAG port. The core can write to and read from On-chip FLASH, which typically holds the firmware. We can use the JTAG port to program the on-chip FLASH through the core access. This constitutes our application type A for utilization of emulation resources: programming of FLASH.

The micro-controller uses its address bus, data bus, and control bus to communicate with other devices on the board or in the system. This system bus interface can be accessed with on-chip emulation functions and can be used to test connections to other devices on the board, such as memories, peripheral interface controllers, and the like. Such Bus Emulation Tests comprise our application type B for the purpose of classifying types of Emulation Tests.

Micro-controllers often include on-chip resources, general purpose I/O, as well as bus interfaces, such as Ethernet ports, USB ports, RS232 or RS485 ports, CAN interfaces, and so on. If the core provides emulation functions to access such internal circuits and interfaces, we can use the JTAG port to initiate "mini functional tests", if you will. This would be an application type C for the utilization of emulation resources.

So, the basic idea is to transform the micro-controller to an embedded test controller for the execution of test operations and FLASH programming, all controlled via the JTAG port.
Let’s say we have a printed circuit assembly with a variety of digital and mixed signal circuitry.

As mentioned, VarioTAP supports the in-system programming of On-Chip and On-Board Flash. This is done through TAP access to the micro-controller emulation functions responsible for the device programming. In case of VarioTAP, the Flash type is automatically identified and the necessary programming algorithm is selected. This provides a unified in-system programming platform for different JTAG compliant micro-controllers that may be used in different designs.

VarioTAP supports NOR Flash and NAND Flash, both On-Chip and external, as well as serial EEPROM. Examples for programming data include a binary image of firmware or test routines, or a serial number, or MAC address, for instance.
VarioTAP also supports the access test of system bus connected devices, based on writing and reading bus data. We call this Bus Emulation Test, which uses emulation functions to execute automated dynamic, at-speed memory access tests, bus device and cluster tests, as well as peripheral I/O tests, while enabling the same pin level diagnostics as boundary scan tests provide.

A special ATPG tool could be used to generate what we call an interlaced JTAG Emulation / boundary scan Interconnect Test with pin diagnostics, essentially testing for board level connectivity with interactions between boundary scan test vectors and Emulation Test vectors. This way we can enhance the structural test coverage for devices which provide a JTAG port and emulation functions with access to I/O pins, but no boundary scan Register.

VarioTAP tests are based on loading Intellectual Property (IP) as well as reading data from and writing data to IP. This also enables user defined tests, even proprietary tests with custom IP.
And the third type of Emulation test applications we refer to as System Emulation Test, which includes the test of On-Chip Interfaces and chip internal resources the emulation functions implemented in the micro-controller have access to.

This System Emulation approach enables a new dimension of test coverage in JTAG/boundary scan applications by supporting protocol driven, fully dynamic tests of board I/O with VarioTAP control of On-Chip Interfaces, for example for the verification of Ethernet, USB, or PCIe ports.

For the test of peripheral interfaces respective tester hardware would be needed to complement the test resources on the UUT, for example a USB client.

VarioTAP also supports the development of custom IP for proprietary on-chip resources and interfaces.

Let's examine a UUT that features a micro-controller with on-chip emulation capabilities, various boundary scan enabled devices such as CPLD’s or FPGA’s, for example, and a range of non-boundary scan devices, including dynamic RAM, Flash, and peripheral I/O circuitry. Obviously, we can apply a set of common boundary scan applications to identify manufacturing defects such as open pins or shorted nets on boundary scan accessible circuit nodes. But in addition to those boundary scan tests, we can also apply VarioTAP tests, utilizing the on-chip emulation functions of the micro-controller for applications such as a dynamic connectivity test to DRAM devices. Furthermore, we can test On-Chip Interfaces and chip internal resources that the emulation functions implemented in the micro-controller have access to. This System Emulation approach enables a new dimension of test coverage in JTAG/boundary scan applications by supporting protocol driven, fully dynamic tests of board I/O with VarioTAP control of On-Chip Interfaces, for example for the verification of Ethernet, USB, or PCIe ports. For the test of peripheral interfaces respective tester hardware would be needed to complement the test resources on the UUT, for example a USB client. This is where VarioCORE comes into play. VarioCORE modules can be connected to the UUT peripheral connectors and can be used as digital I/O modules for boundary scan connectivity tests. In a second test step, the VarioCORE modules can then be reconfigured as functional interface hardware to support mini-functional tests between the VarioTAP controlled on-chip emulation functions in the microcontroller and the peripheral interfaces on the UUT.
A major part of the VarioTAP technology are VarioTAP device models, which have a multi-level architecture with three IP (Intellectual Property) classes, in alignment with the three types of Emulation Test applications we have discussed. IP for internal and external Flash programming includes functions to erase, blank-check, program, and verify Flash memory. Bus Emulation Test IP includes functions to read and write bus data and provides the basis for custom IP designs. Bus Emulation Test IP also enables the automated generation of dynamic memory access tests and bus device tests. IP for System Emulation Tests of on-chip interfaces and resources includes I/O control functions, interface control function, auxiliary control functions, and chip specific functions.

In GOEPEL’s SYSTEM CASCON, Emulation Test and boundary scan can utilize the same programming language, CASLAN. The application flow for VarioTAP emulation tests is the same as for standard boundary scan tests, while the VarioTAP model enables control over the micro-controller’s emulation functions with CASLAN commands. Custom IP is also handled via a CASLAN API.

In such a tester environment, one tester hardware and software handles a variety of micro-controllers, DSP’s, CPU’s, etc. as well as different levels of emulation tests, all in conjunction with boundary scan tests. VarioTAP virtually transforms a micro-controller to provide dynamic pin electronics for the purpose of dynamic board level test applications, as opposed to the quasi-static pin electronics provided by boundary scan registers for the purpose of structural connectivity tests. Furthermore, VarioTAP supports automated test generation for many types of Emulation Tests, providing predictive fault coverage and pin level diagnostics.
**VarioTAP applications**

- Test of Digital I/O
- Test of Analog / Mixed-Signal I/O
- Fast external Flash Programming
- On-Chip Flash Programming
- Test of Bus Interfaces
- Test of Peripheral Circuitry
- Dynamic Memory Access Tests
- Customer specific Tests

- Unique: Interlaced utilization of emulation resources and boundary scan resources
Fault coverage improvements and other benefits

- Boundary scan provides:
  - Embedded test access
  - Deterministic test coverage
  - Very good diagnostics

- JTAG (on-chip) emulation provides:
  - Dynamic fault coverage
  - Verification of circuit functions

Summary of fault coverage improvements and other benefits when utilizing On-Chip Emulation resources and boundary scan for board level test.
**Fault coverage improvements and other benefits**

- VarioTAP combines boundary scan and on-chip emulation to provide:
  - JTAG controlled functional tests
  - Interlaced boundary scan and on-chip emulation tests for extended connectivity tests
  - Automated test generation and deterministic test coverage for (functional) on-chip emulation tests

Summary of fault coverage improvements and other benefits when utilizing On-Chip Emulation resources and boundary scan for board level test
Questions?
Question 1

- Is there a standard defining JTAG / boundary scan resources?
  If so, which standard?

IEEE 1149.1
Question 2

Name potential board and system level test applications supported by JTAG / boundary scan.

- Connectivity test;
- Memory cluster test;
- Logic cluster test;
- In-system programming for CPLD, Flash, serial EEPROM;
- Use of on-chip emulation resources for board level test applications;
- Debug access for verification of circuit functions;
- Etc.
Question 3

What is one of the most important printed circuit board level “design for test” requirements enabling the utilization of boundary scan capabilities implemented in integrated circuits?

- Implement a boundary scan chain: make the TAP accessible.
- Allow compliance enable pattern to be satisfied to enable JTAG / boundary scan compliance.

Implement a scan chain:
connect the TAPs of the various IEEE 1149.1 compliant devices to a daisy-chain and make it accessible for a JTAG / boundary scan test controller.
Thank You!
Contact information

For further information, please:
- Visit our website at www.goepelusa.com
- Contact your local sales representative
- Call us at 1-888-4GOEPEL
- Email us at sales@goepelusa.com
Appendix
References and tools

- White Paper: “Combining Boundary Scan and JTAG Emulation for advanced structural Test and Diagnostics”

- Boundary Scan Coach:
  - software tool demonstrating the key principles of JTAG / boundary scan as defined in IEEE 1149.1

- BSDL Syntax Checker:
  - software for verification of BSDL syntax and semantics

- TAP Checker:
  - software for validation of JTAG / boundary scan implementations in integrated circuits

- CASCON GALAXY:
  - software for device, board, and system level JTAG / boundary scan test and emulation applications