RH850 & RL78 - Next Generation of Automotive Microcontrollers
Renesas Technology & Solution Portfolio
Microcontroller and Microprocessor Line-up

32-Bit High Performance, High Scalability & High Reliability

- Industrial & Automotive, 130nm
- 144µA/MHz, 0.2µA standby

- Industrial & Automotive, 150nm
- 190µA/MHz, 0.3µA standby

- Automotive, 40nm
- 500µA/MHz, 35µA deep standby

8/16-Bit True Low Power, High Efficiency & Integration

- Industrial & Automotive, 130nm
- 350µA/MHz, 1µA standby

- Automotive & Industrial, 90nm
- 600µA/MHz, 1.5µA standby

- Automotive, 40nm
- 500µA/MHz, 35µA deep standby

- Industrial, 90nm
- 500µA/MHz, 1.6µA deep standby

- Industrial, 40nm
- 200µA/MHz, 0.3µA deep standby
‘Enabling The Smart Society’

■ Challenge:
“How to meet the next generation of automotive MCU real time control requirements while at the same time meeting green requirements and “Smart Car” vehicle evolutions which OEMs and consumer are demanding.

■ Solution:
This class will introduce Renesas’ next generation of Automotive MCUs and show they meet demands of vehicle OEMs real time control systems and Green and “Smart car” goals.
Agenda

- Automotive Trends
- Goals for Next Generation MCU Design
- Performance vs. Power Consumption
- Flash Memory Challenges and Renesas Response
- Advance Networking and Security IP
- Functional Safety Considerations
- Roadmaps
Automotive Trends
Macro Trends - Energy

- Lower weight options
- Smaller vehicles
- Architectures considering HEV and electric vehicle options
- More efficient, greener flexible fuel engines
- Stricter Fuel economy standards: (Euro6; CAFÉ)
Macro Trends – Consumer Demand

- More convenience items
- Integrated functions
- More safety and security
- More horse power & better gas mileage
- Intuitive functionality
- Connectivity
Embedded System Trends

- Increase in MCU performance &
- Lower current draw

- Increase in Flash Memory &
- Safety as Value Added

- Advanced Networking &
- Security concerns

Creating Technologies and Designing MCUs Which Meet These Trends is our Challenge!
Goals of the New Generation of 32-bit MCU

**High Performance**
- High performance CPU
- Multi core
- High-speed Flash access
- Better MIPS/mA
- Advanced Peripherals
- Advanced eco-system

**High Reliability**
- Security feature
- Functional safety
- High-temperature operation

**High Scalability**
- Scalable architectures
- Scalable peripherals
- Compatibility from low to high
New Generation of 16-bit MCU

- True Low Power
- Broad Scalability
- High Performance
- Comprehensive Tools And Support
- High Quality And Safety
- System Cost Reduction

* Subject to device
Renesas 16 and 32-bit Automotive MCUs

Performance

32b & 16b Automotive MCU supplier in the World*

#1

Performance and Power Consumption
More Performance – 32-bit CPU Core Roadmap

Succession of “850” Architecture

- **V850E1**
  - 5-stage
  - 7-Stage
  - dual-issue

- **V850E2**
  - 5-stage
  - FPU

- **V850E2R**
  - 7-Stage
  - dual-issue
  - FPU

- **V850E2M**
  - MPU

- **G3M**
  - FPU (IEEE754-2008)
  - Branch prediction
  - SIMD
  - Multi-Core

- **G3K**
  - 5-stage

- **E2S**
  - 5-stage

High Performance and Low power

Good Performance and Low Power
G3M & G3K 32-bit core characteristics

G3M- Real-time supports w/ improved data processing performance

G3K- Small core with high performance and low-power

7 Stage Dual issue Pipeline (G3M)

5 Stage Pipeline (G3K)

- Optimized pipeline structure CPU Freq.

Difference of ISA

ISA: Instruction Set Architecture
RH850 Architecture (Example CPU Core and Pipeline)

Example RH850 CPU

- 96 MHz CPU Core 2.x DMIPS/MHz
- Memory Protect Unit
- 32x 32bit General Purpose Registers
- 32bit Floating Point Unit (Optional)
- 32x32 +64 MAC, 64b Result
- 32 x 32 DIV or MULT, 32bit or 64bit Result
- Interrupt Control
- On-Chip Debug

- 5-STAGE PIPELINE

- Achieves: One Clock-Per-Instruction (CPI)

HARVARD ARCHITECTURE

- Flash Memory
  Capable to Flash 120 MHz

- SRAM

- 128 bit path Instruction
- 39 bit path Operand (Data)

- Instruction Queue
- Data Queue

- Capable to Flash 120 MHz
RH850 Architecture ... System Interface

- **RH850 MCU**
  - Flash Memory, up to 120MHz Access
  - SRAM, up to 120MHz Access

- **Bus Master**
  - Instruction: 128b
  - DATA: 32b

- **Internal Main Bus & System interconnect**
  - 32 bits

- **Peripheral Busses to Spread Bandwidth Loading**
  - DMAC (bus master)

- **Communication (CSI, CAN, SCI, LIN, I2C, Flex Ray)**

- **Timers (TAUA, TAU J, OST, CMT)**

- **Analog**

- **GPIO**

- **System Control (DMA, E2P, ICU, LVD, RTC, WDG, CLKS)**

- **BUFFER**
  - 128b INST
  - 32b DATA
  - 64 bits

- **RH850**
32-bit Multi-Core Architectures for Automotive

**Scalable core for both performance and safety**

- **CPU 1**
- **CPU 2**
- **CPU 1’**
- **CPU 2’**

Double Redundant Core ("Quad Core")

- **Redundant Core**
- **Redundant + Performance Core**

- **Single Core**
- **Dual Core**
- **Triple Core**
RH850: 40nm MCU Series for Vehicle Control

**Powertrain**
- High: 320MHz Dual core w/ Lockstep I/O CPU
- Mid: 240MHz Dual core w/LS I/O processor
- Low: 160MHz Single core w/LS

**EV/HEV**
- High: 240MHz Dual core w/ LS
- Mid: 240MHz Single core w/ LS
- Low: 160MHz Single Core

**Chassis & Safety**
- High: 240MHz Dual core w/LS x2
- Mid: 240MHz Single core w/ LS
- Low: 160MHz Single Core

**Air Bag**
- High: 240MHz Single core w/ LS
- Mid: 100 MHz Single core Low Power
- Low: 80MHz Single Core Low Power

**Body**
- High: 120MHz Multi Core Low Cyclic Power
- Mid: 120 MHz Single Core Low Power
- Low: 80 MHz Single Core Low Power
Low Power Consumption – RUN Mode

- RH850: No. 1 in power consumption for Run Mode

<table>
<thead>
<tr>
<th>Frequency</th>
<th>PPC 90nm (mA Typ.)</th>
<th>RH850 40nm (mA/MHz)</th>
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<tbody>
<tr>
<td>64MHz</td>
<td>70</td>
<td>0.3</td>
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<tr>
<td>80MHz</td>
<td>30</td>
<td>0.5</td>
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DeepSTOP

- F1x estimated current consumption (typ)
  - STOP mode: 200uA – Done through Clock Gating
  - Deep STOP: 35uA – Utilizing Power Domain
    - ISO area is powered off in Deep STOP

[Bar chart showing current consumption with only 17.5% current]
Low Power Consumption - Standby Mode

- RH850: Excellent power consumption for Low Power Mode, Cyclic Wake Up

<table>
<thead>
<tr>
<th>Avg uA</th>
<th>Description</th>
<th>Reference</th>
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<tbody>
<tr>
<td>210</td>
<td>200uA Target</td>
<td>F1L - Cyclic 50 ms digital &amp; analog IO and UART/LIN evaluation.</td>
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<tr>
<td>180</td>
<td></td>
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<tr>
<td>150</td>
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<tr>
<td>120</td>
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<td>90</td>
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<tr>
<td>60</td>
<td></td>
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<tr>
<td>30</td>
<td>40uA Target</td>
<td>F1L - Cyclic 50 ms digital &amp; analog IO scan.</td>
</tr>
</tbody>
</table>
Low Power Sampling Feature - DeepSTOP

Digital switches

Port Polling

CPU

VCC

DPO

CNTR

COMPARE

Wake CPU?

yes

Analog Polling

APO

CNTR

Range

Analog

COMPARE

Timer

Analog switches
Leading Edge of RL78 Low Power

- Lower Power technology
  CPU, Flash, System
- Low Active power
  As low as 66uA/MHz
- Low standby power
  0.49uA (STOP + 32kHz + RTC)
  0.32uA (STOP + LVD)
- Low power peripherals
  LVD, RTC, WDT
- Wake up from standby
  19.1 usec
- Long interval capability
  0.5sec to 1 month
- SNOOZE mode
  ADC, UART/CSI(SPI)
Low Power: Fully Configurable

- Multiple Power Reducing Modes
  - Halt (DMA and all peripherals available)
  - Snooze (ADC, CSI/UART active)
  - STOP (RAM Retained)
Low Power: Snooze Mode Example (ADC)

- ADC operation during standby state
  - 4 comparison criteria: within/outside window, higher/lower than limit
  - Over 30% reduction in power vs. standard ADC operation

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ADC values out of range: Wake up the CPU and process the results
Flash Memory Challenges
Flash Memory Trends

**Flash Requirements are Doubling Approximately Every Five Years**

- Body Control Modules
- Engine Control Modules
- Restraint Control Modules
World First 40nm Flash MCU for Automotive

Leading Flash Process for Next Generation Automotive MCUs

320 MHz CPU
120 MHz Flash
~ 8 MByte
Lowest power consumption

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<tr>
<th>Technology node</th>
<th>100</th>
<th>80</th>
<th>60</th>
<th>40</th>
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<tr>
<td>Transistor / mm²</td>
<td>90nm</td>
<td>65nm</td>
<td>55nm</td>
<td>40nm</td>
</tr>
<tr>
<td>Previous generation</td>
<td>Other Option B</td>
<td>Other Option A</td>
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</table>
Renesas Response to this Flash Growth

**Current Product**

- **V850/Fx4**
  - 256KB to 2MB

- **V850/Px4**
  - 512KB to 2MB

- **SH2A**
  - 1MB to 4MB

- **78K0R/R8C**
  - Up to 256K

**Next Gen**

- **RH850/F1x**
  - 256KB to **8MB**

- **RH850/P1x**
  - 512KB to **8MB**

- **RH850/E1x**
  - 1MB to **8MB**

- **RL78/F1x**
  - Up to **512K**
Advanced Networking and Security
Growth in In-Vehicle Networks

# Nodes in Automotive

- **CAN**
- **MOST**
- **FlexRay**
- **Ethernet**

**Sources:**
- Strategy Analytics, Automotive High Speed Bus Networks January 2012

*2014 SA Data;
**REA estimate based on Market knowledge.

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### Renesas Response to this Network Growth

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<td>Up to 12 Ch</td>
<td>up to 16 Ch</td>
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<tr>
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<td>Up to 3 Ch</td>
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<td>Up to 2 Ch</td>
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<td>1 Unit (2ch/Unit)</td>
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<th>FlexRay</th>
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<td></td>
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<td></td>
<td>1 Ch</td>
<td>1 Ch</td>
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</table>
**LIN**

- Channels which support Master mode only
  - Dedicated H/W LIN peripheral
  - Detection of synch break, bus collision, timeout

- Channels w/ Master mode and Slave mode
  - Master mode same s/w control architecture as above
  - Addition of Slave mode capability

**LIN Bus**

- Break Field
- Synch Field
- ID 0
- Data 1
- Data n
- Check Sum

**LMA interrupts**

- eliminate intermediate interrupts
- only 1 interrupt per message
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CAN

- CAN Channels with Flexible Message Buffer Structure
  - CAN2.0B Active standard ISO11898-1
  - Advanced message filtering capabilities
  - Flexible receive message buffers settings
    - up to 320 reception message buffer
  - 16 transmit buffers per CAN Channel
  - Programmable Gateway routing for each channel
  - Automatic transfer block messages: 16 → 8
  - CAN time stamp output function

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<thead>
<tr>
<th>ch</th>
<th>TX (Dedicated)</th>
<th>RX (Common)</th>
<th>TX / RX (Common)</th>
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<tr>
<td>0</td>
<td>16msg</td>
<td>80msg</td>
<td>240msg (48msg x 5)</td>
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<td>1</td>
<td>16msg</td>
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<td>2</td>
<td>16msg</td>
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<tr>
<td>3</td>
<td>16msg</td>
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<tr>
<td>4</td>
<td>16msg</td>
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</table>
FlexRay™ – Active Safety Examples
Security Concerns Increasing

How to protect my virtual dashboard design?

How to protect against illegal tuning?

How to protect the odometer?

How to secure radio communications?

How to secure the remote entry system and the immobilizer?

How to secure the car diagnosis?

Toward a distributed in-vehicle security system
Two Emerging Standards for Security

- Secure Hardware Extension (SHE): an *low cost on-chip* extension within a MCU which provides:
  - A set of cryptographic services available to the application layer
  - Complete isolation of the secret keys and certificates from the rest of the MCU resources
  - SHE: released in April 2009 as a public specification endorsed by the German OEM consortium “HIS – Hersteller Initiative Software

- EVITA (**E**-safety **V**ehicle Intrusion pro**T**ected **A**pplications)
  - A collaborative research project with partial funding from the European Commission (EC).
  - The EVITA project defines the concept of a Hardware Security Module (HSM) incorporated into Automotive MCUs.
Introducing Intelligent Cryptographic Unit (ICU)

- Two ICU types coexist to address different application needs
  - **ICU-S**: slave unit offering symmetric cryptographic services
  - **ICU-M**: master unit offering asymmetric cryptographic services

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**IP Complexity & Cost**

- ICU-S
  - "SHE" compliant IP
  - Slave unit
  - Private key cryptography
  - Control logic

- ICU-M
  - "EVITA HSM" type-of IP
  - Master unit
  - Private key cryptography
  - Public key cryptography
  - Dedicated CPU
Functional Safety
Functional Safety


- This standard is the “adaption of IEC61508 to comply with needs specific to the application sector of electrical and/or electronic (E/E) systems within road vehicles

- This standard provide normative guidelines on:
  - Automotive safety lifecycle (organization, development, production and EOL).
  - Assign specific Automotive Safety Integrity levels (ASIL) based on a risk based methodology
  - Based on ASIL level assign specific requirements to be met
  - Method on validating
  - Requirements for relations with suppliers
Involvement of ISO26262 work products in Renesas standardized development process for MCU has been completed.
Development Process for LSI (SEooC)

- Safety goal
- Functional safety concept, (FSR, preliminary architectural assumption)
- Technical safety concept, (TSR, System design)
- Device safety concept (Assumed device TSR/HSRS, device design, Assumptions related to the design external to device)
- Device safety verification (Verification of consistency and completeness between requirement and design)
- Device testing
- Device safety plan
- Device safety assessment
- Decision for ASSP
- Validation for the system

Requirement derivation and design for system (OEM/Tier1)

Requirement derivation and design for device (device vendor)

System verification and validation (OEM/Tier1)

Product verification and validation (MCU vendor)
Platform Functional Safety Features

Example of features available or under consideration

- ECC on memories
- Clock Monitors
- POC / LVI
- MPU, PPU
- Peripheral Diagnostics
  - ADC, CSI/UART loopback
  - ... (t.b.d.)

QM

ASIL A/B

- ECC on memories
- Clock Monitors
- Error Management
- Software self tests
- POC / LVI
- MPU
- Peripheral Diagnostics
  - ADC, CSI/UART loopback
  - ext./int. intelligent WDT
- SW CST
- SW ROM / RAM test
- SW Peripheral Tests
- AUTOSAR ASIL B
- Compiler ASIL B
- Tools

ASIL C/D

- Redundant Core Lockstep
- Error Management
- Logic / Memory BIST
- ECC on memories
- Clock Monitors
- Memory Patrol
- POF / LVI
- MPU, Timing Supervision,
  - Peripheral Diag./protection
    - ADC, CSI/UART loopback
  - ... (t.b.d.)
- AUTOSAR ASIL D
- Compiler ASIL D
- Tools
Roadmaps
RH850F1x for Body

1. **Extreme Low Power consumption**
   - Low power operation at 0.5mA/MHz at single core
   - Dual core for High-end for low power & performance
   - Enlarge battery life time in standby mode

2. **Full coverage of Body Networking**

3. **Hardware Security module**
   - Hardware Security Support to meet “SHE” (Secure Hardware Extension) and Evita concept. Standardization in HIS consortium

4. **Wide Line-up to cover various body systems**
   - Memory range: 128KB to 8MB Flash memory
   - Package range: 48pin to 357pin
1. **Extreme Low Power consumption**
   - Low power operation at 130uA/MHz at single core
   - Special Snooze mode or Cyclic power applications

2. **Ideal for LIN Slave and single / dual CAN**

3. **High Temperature support for Engine Compartment**
   - Support for 150°C Ambient condition

4. **Wide Line-up to cover various body systems**
   - Memory range : 8KB to 512KB Flash memory
   - Package range : 20pin to 144pin
MCU Roadmap for Body

2007

Gateway
- 32 - 160MHz
- 256KB - 8MB
- 1 - 6 CAN
- FlexRay / Ethernet

V850/CAG4-M

V850/Fx4-H

V850/Fx4

2009

V850/Fx3

V850/Fx3-L

M16C

R32C

2011

RH850/F1x

1 - 6 CAN

FlexRay / Ethernet

2013

2015

BCM

Stand Alone ECU
- 20 - 80MHz
- 64KB - 2MB
- 1 - 6 CAN

V850/Fx4-L

V850/Fx4

V850/Fx4-H

Gateway

Dedicated ECU
- 16 - 32MHz
- 32 - 512KB
- 0 - 2 CAN

78K0/Fx2&Kx2

78K0R/Fx3

78K0S/Kx1+

1 - 6 CAN

78K0/Fx2-L

M16C

R8C/2x

R8C/3x

R8C/5x

RH850/F1x
ASIL D capable

- Lock step dual core (LSDC) for ASIL-D functional safety requirement
- Scalable LSDC line up for Chassis & Safety applications (240MHz to 80MHz)
- Safety mechanism to reduce software and system overhead

ASIL B capable

- Cost conscious solution for ASIL-B functional safety requirement
- Single core with hardware measures & software core self test
- Combining RH850 R1x + System base chip to realize ASIL-D capable system

RENESAS Expertise
Functional Safety

Standardisation Activities
- IEC61508
- ISO26262

Enough experience of functional safety

Work products Required for LSI
Support and Solutions for Effective development
## MCU Roadmap for Chassis & Safety

### Integrated Safety Unit
- **High End Chassis controller**
  - 200-300MHz / 2-4MB

### Stability Control
- **High EPS**
  - 160-240MHz
  - 1M-2MB

- **EPS/Braking**
  - 160MHz
  - 512KB -1MB

### ABS/ Airbag
- 80MHz /256KB-512KB

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<td>V850 / PG2</td>
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<td>V850 / Fx4</td>
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<td>V850 / Fx4-L</td>
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<td>RH850/P1x</td>
<td>Ultra-High</td>
<td>240MHz</td>
<td>LSDC x 2</td>
<td>240MHz, LSDC+PCU</td>
<td>240MHz, LSDC+PCU</td>
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<td>RH850/P1x</td>
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<tr>
<td>RH850/P1x</td>
<td>Mid-Range</td>
<td>80/160MHz, LSDC</td>
<td>80/160MHz, LSDC</td>
<td>80/160MHz, LSDC</td>
<td>80/160MHz, LSDC</td>
<td>80/160MHz, LSDC</td>
</tr>
<tr>
<td>RH850/P1x</td>
<td>Mid-Low</td>
<td>80MHz, LSDC</td>
<td>80MHz, LSDC</td>
<td>80MHz, LSDC</td>
<td>80MHz, LSDC</td>
<td>80MHz, LSDC</td>
</tr>
<tr>
<td>RH850/R1x</td>
<td>80MHz, Single Core</td>
<td>80MHz, Single Core</td>
<td>80MHz, Single Core</td>
<td>80MHz, Single Core</td>
<td>80MHz, Single Core</td>
<td>80MHz, Single Core</td>
</tr>
</tbody>
</table>

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**LSDC:** Lock step dual
1. High Performance & Safety
   - 4 CPUs (Dual CPU Core / Lock Step Dual / Peripheral CPU)
   - 320MHz Main CPU operation
   - ASIL-D capable for Functional Safety with Lock Step Dual

2. Dedicated Hardware for Power train
   - Advanced Timer Unit
   - Autonomous Pulse Adaptor (APA) for Direct Injection
   - Digital Filter Engine (DFE) for knock detection
   - \( \Delta \Sigma \) Analog Digital Convertor

3. Scalability for downsizing
   - Software compatibility from High-end to Low-end
   - High-end at 320MHz/8MB flash to Low-end at 80MHz/1MB flash

4. High temperature operation
   - \( T_j = 170 \) degC max. (KGD)
MCU Roadmap for Power train

---|---|---|---|---
> 240MHz | > 4MB | | | 

~ 200MHz | ~ 4MB | | | 

~ 160MHz | ~ 2MB | | | 

~ 80MHz | ~ 1MB | | | 

SH7059  | 80MHz | 1.5MB | | 

SH7058S  | 80MHz | 1MB | | 

V850/GP4  | 80MHz | 1MB | | 

GP8  | 80MHz | 512kB | | 

SH72543R  | 200MHz | 2MB | | 

SH72546R  | 200MHz | 3.75MB | | 

SH72544R  | 200MHz | 2.5MB | | 

SH72567R  | 200MHz | 4MB | | 

SH72531  | 120MHz | 1.25MB | | 

SH72533  | 160MHz | 2MB | | 

SH72544  | 200MHz | 3.75MB | | 

SH72546  | 200MHz | 4MB | | 

SH72567  | 40nm | | | 

RH850/E1x  | 240~320MHz x2core | 8MB Flash | | 

RH850/E1x  | ~240MHz x2core | 4MB Flash | | 

RH850/E1x  | 160MHz | 2MB Flash | | 

RH850/E1x  | 80MHz | 1MB Flash | | 

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Next Gen. MCU for HEV/EV

1. **High Performance & Safety**
   - **3 CPUs** (Lock Step Dual / Peripheral CPU)
   - 240MHz Main CPU operation
   - **ASIL-D capable** for Functional Safety with Lock Step Dual

2. **Dedicated Hardware for Motor Control**
   - Cost effective built-in **Resolver Digital Converter** (collaboration with Tamagawa-Seiki)
   - Less CPU load Built-in **Enhanced Motor Control Timers**
   - **2 motor controllable** by 1 MCU

3. **Scalability for downsizing**
   - **Software compatibility** from High-end to Low-end
   - High-end up to 240MHz/4MB Flash

4. **Wide Line-up to cover various HEV/EV systems**
   - Motor / Generator, DC/DC, Vehicle control & Battery management
MCU Roadmap for HEV/EV

- **2007**
  - MG (Motor Generator)
    - SH7227-1MB
  - DC/DC
    - V850/PG2
      - 240/496KB
  - Vehicle Control
    - V850/Fx3
  - Battery Management
    - V850/Fx3

- **2009**
  - MG (Motor Generator)
    - SH7227-1MB
  - DC/DC
    - V850/Px4
      - 512/384KB, LSDC
  - Vehicle Control
    - V850/Fx4-Motor
  - Battery Management
    - V850/Fx3

- **2011**
  - MG (Motor Generator)
    - SH7227-1MB
  - DC/DC
    - V850/Px4
      - 1MB, LSDC, RDC-IF
  - Vehicle Control
    - V850/Fx4-Motor
  - Battery Management
    - V850/Fx4-H
    - V850/FK4-G
    - V850/Fx4

- **2013**
  - RH850/C1x
    - 2RDC-IF, 4MB, 320MHz, LSDC+1CPU+PCU
  - RH850/x1x
    - 1RDC-IF, 2MB, 240MHz, LSDC+PCU

- **2015**
  - RH850/P1x
  - RH850/F1x
Questions?
‘Enabling The Smart Society’

**Challenge:**
“How to meet the next generation of automotive MCU real time control requirements while at the same time meeting green requirements and “Smart Car” vehicle evolutions which OEMs and consumer are demanding.

**Solution:**
“Renesas’ next generation RL78 and RH850 Automotive MCU for real time embedded control will meet the demands of advanced vehicle architectures and support the “smart society” consumer demands.

Do you agree that we accomplished the above statement?