V850 Architecture Overview

High performance and Energy Efficient

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Agenda

- V850 Positioning among the REA Products
- V850 MCU family
  - Naming convention
  - Product family
- V850ES Architecture for Performance
  - Pipeline enhancements
  - Instruction enhancement
- V850ES Low Power and Energy Efficiency
  - High performance at low freqency
  - Flexible standby modes

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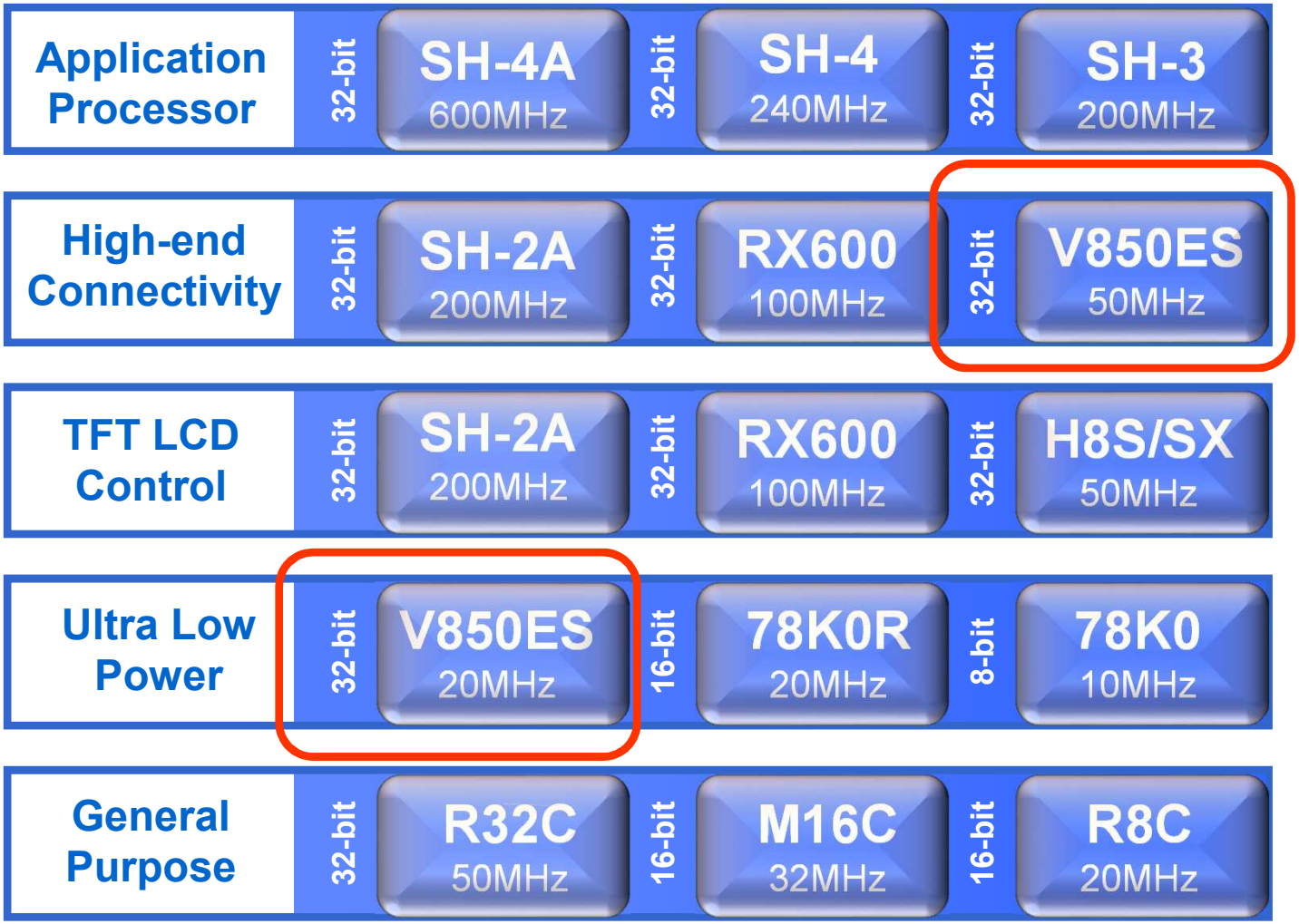
MCU and MPU Solutions



Application Focused Solutions

WiFi	Motor Control	Capacitive Touch	Industrial CAN	Lighting
SH, RX, R8C	SH, RX, R8C	R8C	R8C, R32C, SH	78K0

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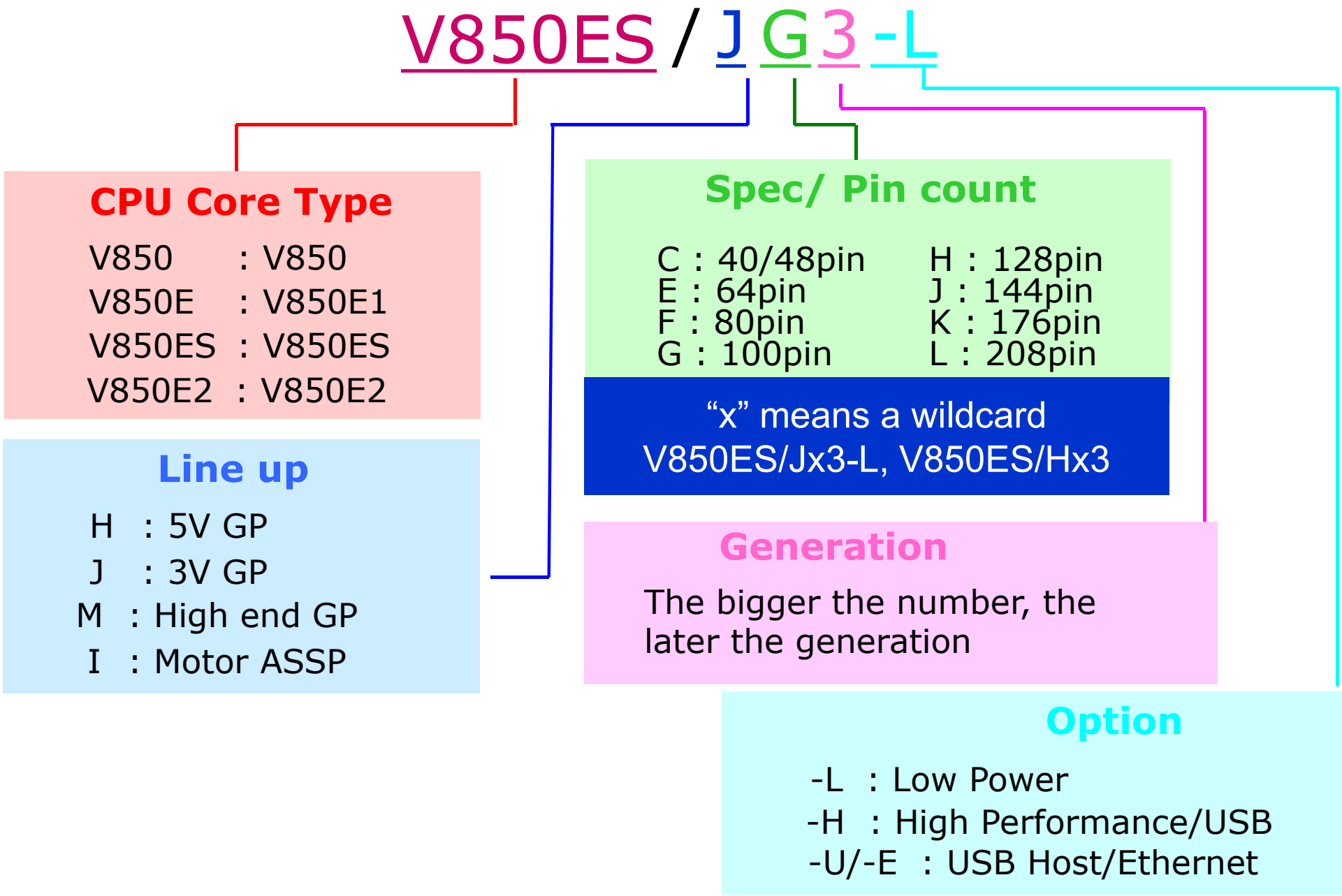
MCU Naming Convention



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V850 MCU Products in 2010

General Purpose

V850ES/Jx3
62 DMIPS v2.1

Max Freq: 32MHz
Voltage: 2.85 – 3.6V
Pins: 100-144
Flash: 385-1024 KB
RAM: 32-60 KB

Ultra Low Power General Purpose

V850ES/Jx3-L
STOP Current 1.5uA

Max Freq: 20MHz
Voltage: 2.0 -3.6V
Pins: 80 - 100
Flash: 256 - 512KB
RAM: 32 - 40KB

Low Power Connectivity

V850ES/Jx3-L
USB Device

Max Freq: 20MHz
Voltage 2.85-3.6V
Pins: 100
Flash: 256 - 512 KB
RAM: 40 KB

Connectivity

V850ES/Jx3-H
81 DMIPS v2.1
USB Device

Max Freq: 48MHz
Voltage: 2.85-3.6V
Pins: 48 -128
Flash: 16-512 KB
RAM: 8-56KB

V850ES/Jx3-U
81 DMIPS v2.1
USB Device + Host

Max Freq: 48MHz
Voltage 2.85-3.6V
Pins: 100-128
Flash: 384-512 KB
RAM: 48-56KB

V850ES/Jx3-E
84 DMIPS v2.1
Eth MAC + USB Device

Max Freq: 50MHz
Voltage: 2.85-3.6V
Pins: 128-144
Flash: 256-512 KB
RAM: 76-128KB

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What is unique about V850 MCUs?

High performance in Small Package

V850ES delivers 1.9DMIPS/MHz as small as 7x7mm 48-pin package

Energy Efficient for Portable Application

V850ES/Jx3-L delivers 0.3mA/DMIPS

Flexible sleep and wake up for portable application

Radio can wake up sleeping V850 by sending data/clock on CSI

Fast Response Time for control

Minimum 4 cycles compared to Cortex-M3 12 cycles[1]

High density Flash with automotive reliability

Transparent Error Correction Code embedded in flash

[1] Source: http://www.arm.com/products/processors/cortex-m/cortex-m3.php

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V850ES MCU Architecture
High Performance and Low Power

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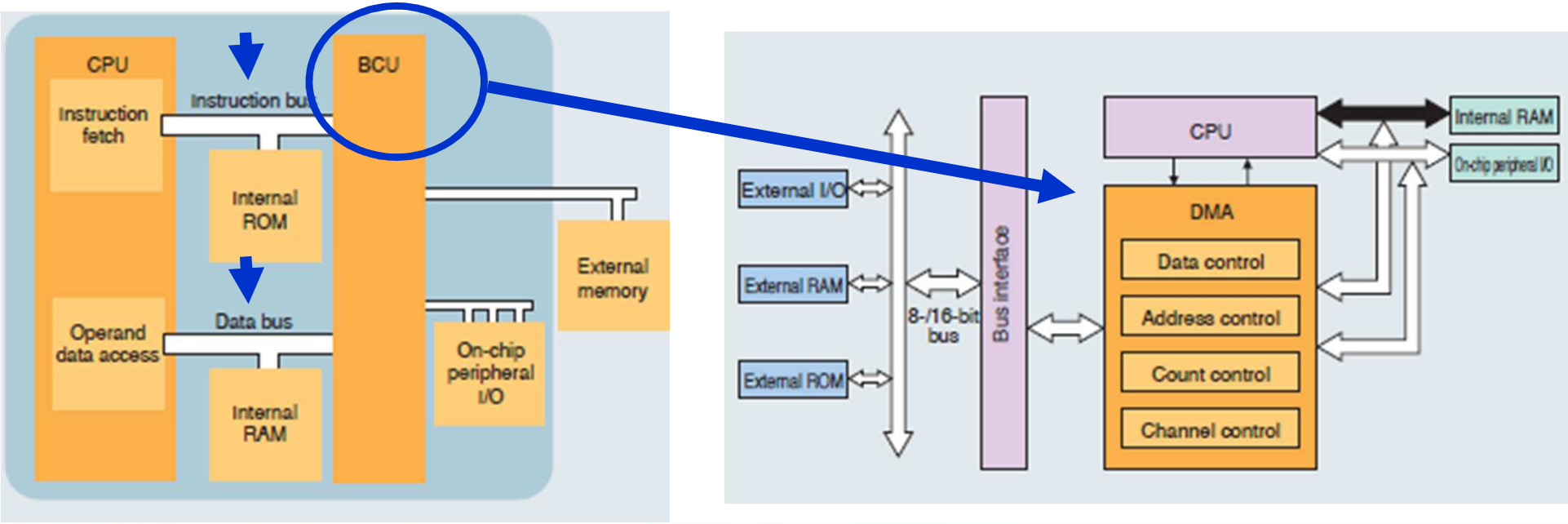
V850 Architecture

- Harvard Architecture
  - Separate Instruction and Data buses to reduce congestion from the von Neumann architecture single bus architecture
- Bus Control Unit with DMA
  - Data transfer without MCU intervention
  - MCU can continue execution – increase performance
  - DMA bring data in/out – increase bandwidth



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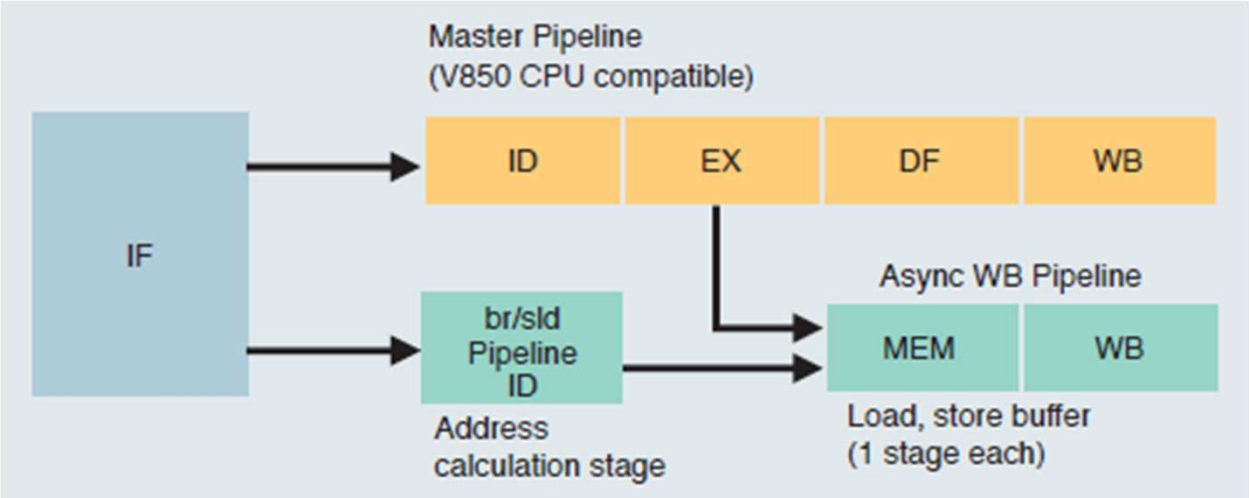
Enhanced Pipeline Delivering High Performance

- Enhanced 5-stage pipeline with Branch/Load Pipe and Non-Block Load/Store delivering 1.9DMIPS/MHz



- Branch address can be calculated in ID stage to reduce typical branch penalty

- Load/store buffer hide 1 clock cycle memory latency

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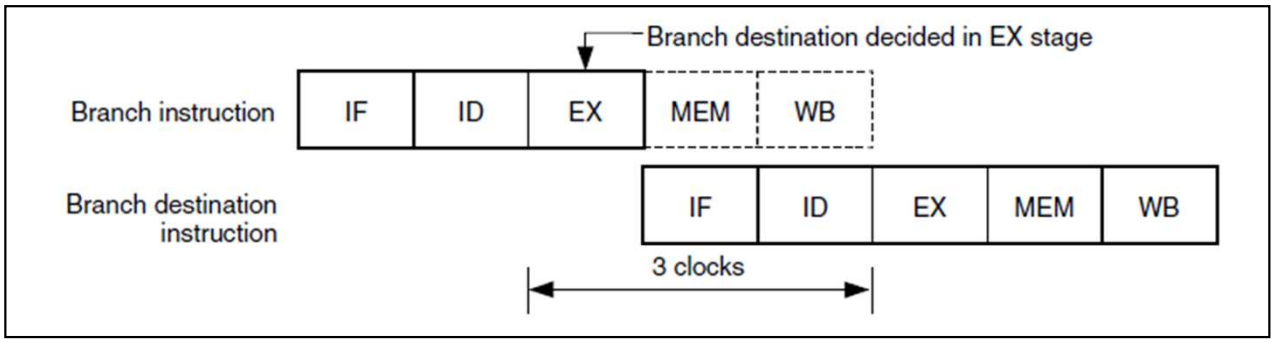
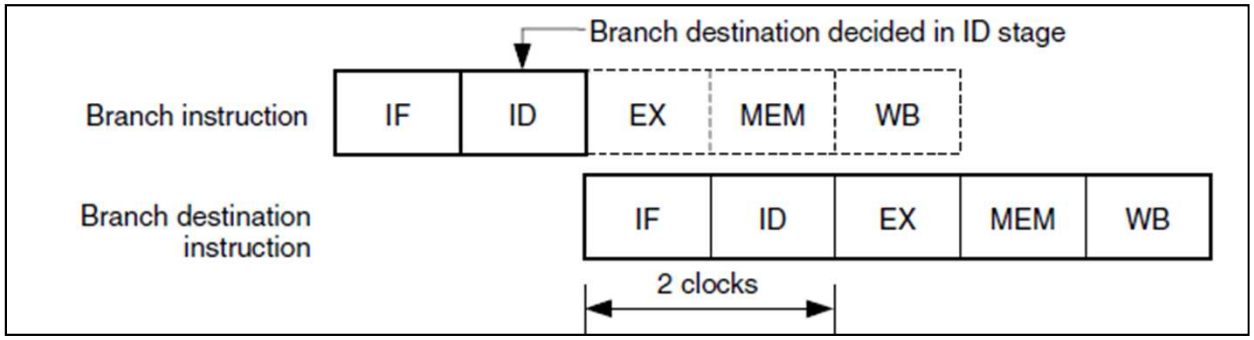
Branch/Load Pipe hides latency

- Typical BEQ instruction: BEQ REG1, REG2, Immediate
  - Compare REG1 and REG2 in ALU (EX stage)
  - Address calculation can only be done in EX stage



- V850 Conditional Branch: BCOND Immediate
  - Branch using Flag such as Zero, Carry, Negative and etc
  - Address calculation is done in ID stage



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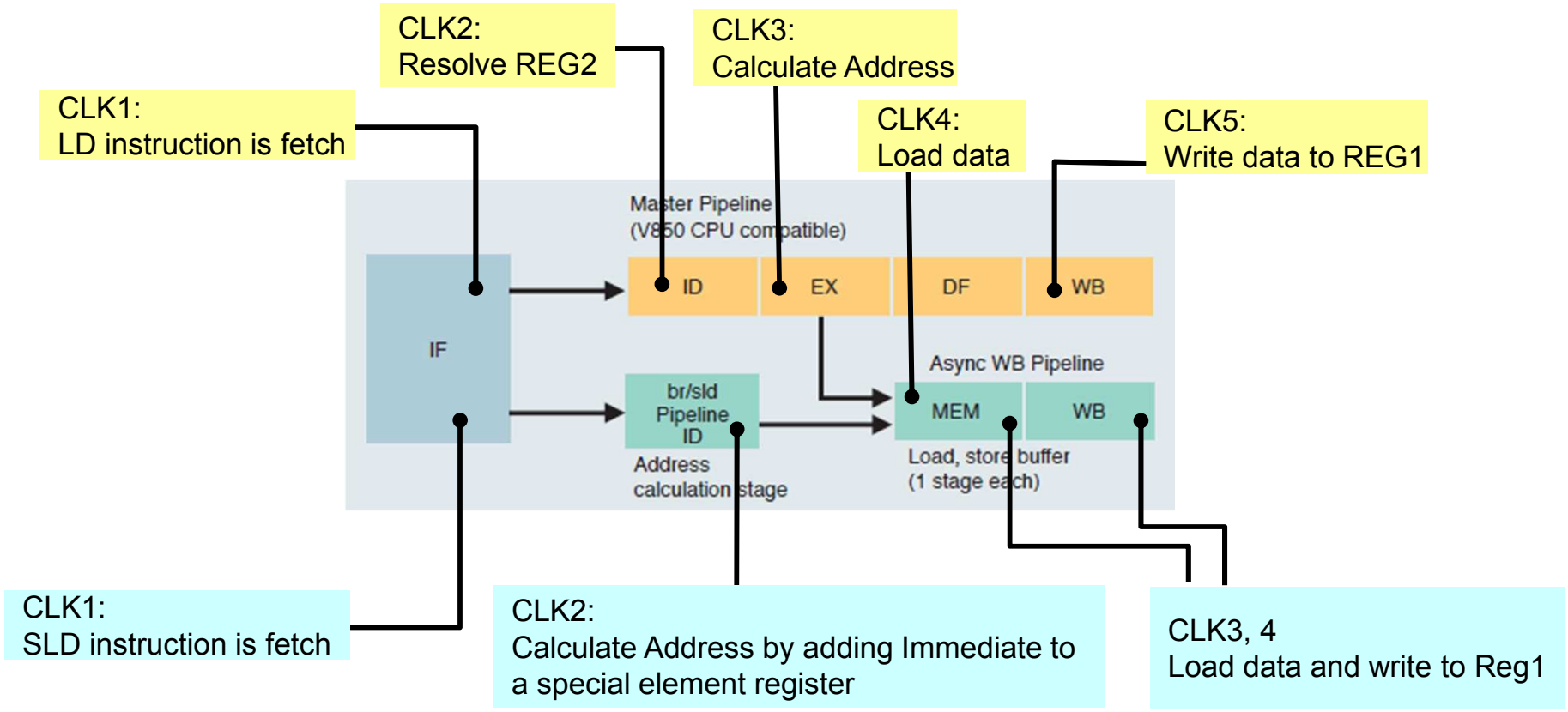
Branch/Load Pipe hides latency

- Typical LOAD instruction: LD REG1, REG2, Immediate



- V850 Short LOAD instruction: SLD REG1, Immediate

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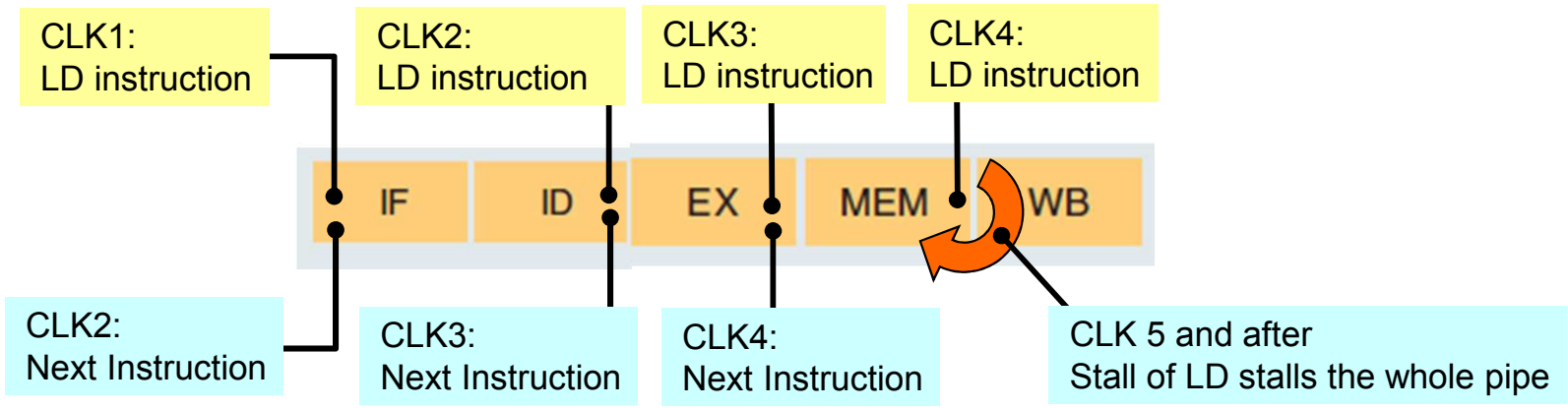
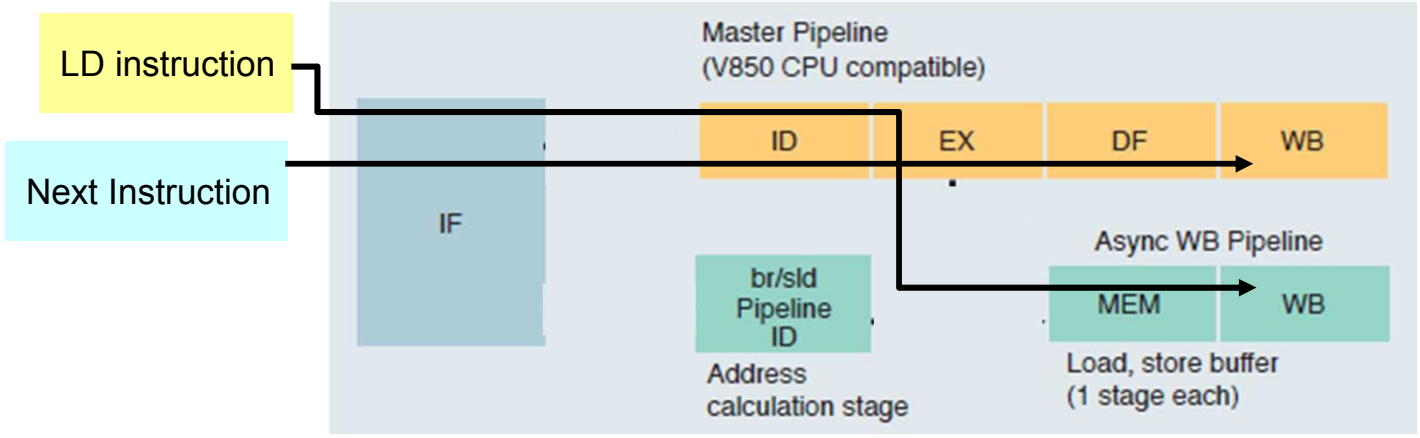
Load/Store Buffer reduces stalling pipe

- Load/store stalls a traditional RISC 5-stage pipeline



- Enhanced load/store buffer reduces pipeline stall



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Instruction Set For Performance and Fast Control

- Fast computation
  - Saturated arithmetic operation
  - 16x16 hardware multiplier to support fast multiplication
  - Single cycle shift with barrel shift hardware
  - Single cycle bit manipulation operation
  - Single cycle byte swap

- Fast Response
  - Conditional Branch
    - Branch based on Flag (C, Z and etc) hide 1 clock latency
  - Table of Function Call
    - Faster address calculation for long call

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Low Power Consumption

- Enhanced pipeline delivers high performance at 1.9DMIPS/MHz (v2.1)
- V850ES can operate at a low frequency to achieve the same processing performance as Cortex-M3 (1.25 DMIPS/MHz) [1]
- Lower frequency consumes less power

	DMIPS (2.1) DMIPS/MHz	CPU Freq. [2]	Flash Freq. [2]	DMIPS (2.1) [3]	Run Current 3.3V 25C[2]
A Cortex-M3 based MCU	1.25	36MHz	24 MHz (1 wait state @ 36MHz) (max Flash freq = 24MHz)	40 DMIPS	17.3mA
V850ES/Jx3-L	1.95	20MHz	20 MHz (0 wait state) (max Flash freq = 32MHz)	39 DMIPS	12mA

1 Source: http://www.arm.com/products/processors/cortex-m/cortex-m3.php
2 Based on values stated in an MCU vendor's Cortex M3 based MCU datasheet
3 Based on internal benchmarking

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[1] Source: http://www.arm.com/products/processors/cortex-m/cortex-m3.php
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[3] Based on internal benchmarking

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Different Standby Modes and Options

- Different operation modes to tailor application needs

[2] 32kHz oscillator/PLL can be switched on/off

Mode	Condition								
	32kHz Osc. Ckt.	Main Osc. Ckt.	PLL	CPU	Peripherals		Regulator	Flash	RAM/Register
					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained

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					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained
HALT	ON[2]	ON	ON[2]	STOP	ON	ON	ON	ON	Retained

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Different Standby Modes and Options

- Different operation modes to tailor application needs

[1] RTC and some peripherals such as UART can be left on
[2] 32kHz oscillator/PLL can be switched on/off

Mode	Condition								
	32kHz Osc. Ckt.	Main Osc. Ckt.	PLL	CPU	Peripherals		Regulator	Flash	RAM/Register
					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained
HALT	ON[2]	ON	ON[2]	STOP	ON	ON	ON	ON	Retained
IDLE1	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	ON	Retained

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					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained
HALT	ON[2]	ON	ON[2]	STOP	ON	ON	ON	ON	Retained
IDLE1	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	ON	Retained
IDLE2	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	OFF	Retained

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	32kHz Osc. Ckt.	Main Osc. Ckt.	PLL	CPU	Peripherals		Regulator	Flash	RAM/Register
					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained
HALT	ON[2]	ON	ON[2]	STOP	ON	ON	ON	ON	Retained
IDLE1	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	ON	Retained
IDLE2	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	OFF	Retained
STOP	ON[2]	STOP	STOP	STOP	STOP[1]	STOP[1]	Low Power	OFF	Retained

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Different Standby Modes and Options

- Different operation modes to tailor application needs

[1] RTC and some peripherals such as UART can be left on
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	32kHz Osc. Ckt.	Main Osc. Ckt.	PLL	CPU	Peripherals		Regulator	Flash	RAM/Register
					RTC	Others			
RUN	ON[2]	ON	ON[2]	ON	ON	ON	ON	ON	Retained
HALT	ON[2]	ON	ON[2]	STOP	ON	ON	ON	ON	Retained
IDLE1	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	ON	Retained
IDLE2	ON[2]	ON	ON[2]	STOP	STOP[1]	STOP[1]	ON	OFF	Retained
STOP	ON[2]	STOP	STOP	STOP	STOP[1]	STOP[1]	Low Power	OFF	Retained
RTC Backup (Jx3-L, with 384KB or up)	ON	STOP	STOP	STOP	ON	STOP	OFF	OFF	Only RTC Registers

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Comparison to a Cortex-M3-based MCU

	DMIPS (2.1) DMIPS/MHz	CPU Freq. [1]	Flash Freq. [1]	DMIPS (2.1) [2]	Run Current 3.3V 25C[1]	Energy Efficiency
A Cortex M3-based MCU	1.25	36MHz	24 MHz (1 wait state @ 36MHz)	40 DMIPS	17.3mA	0.4mA/DMIPS
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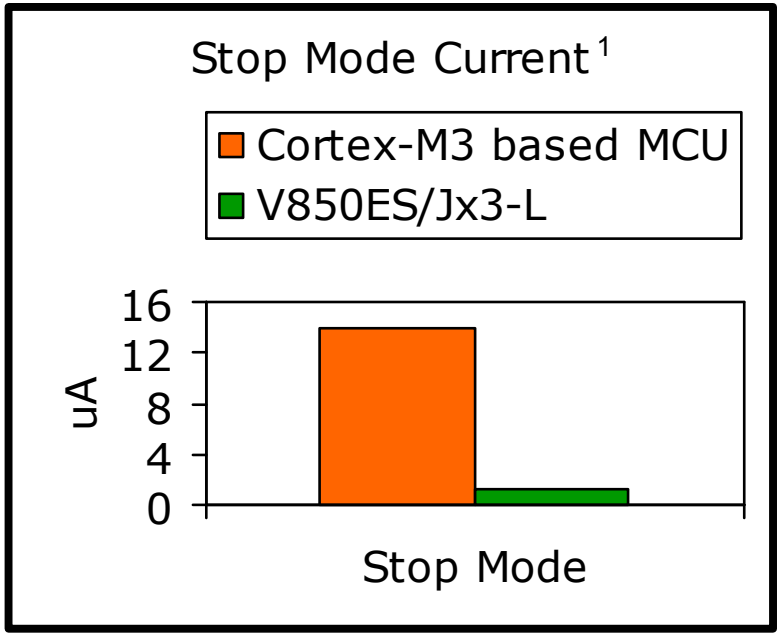

1 Based on values stated in an MCU vendor's Cortex M3 based MCU datasheet
2 Based on internal benchmarking

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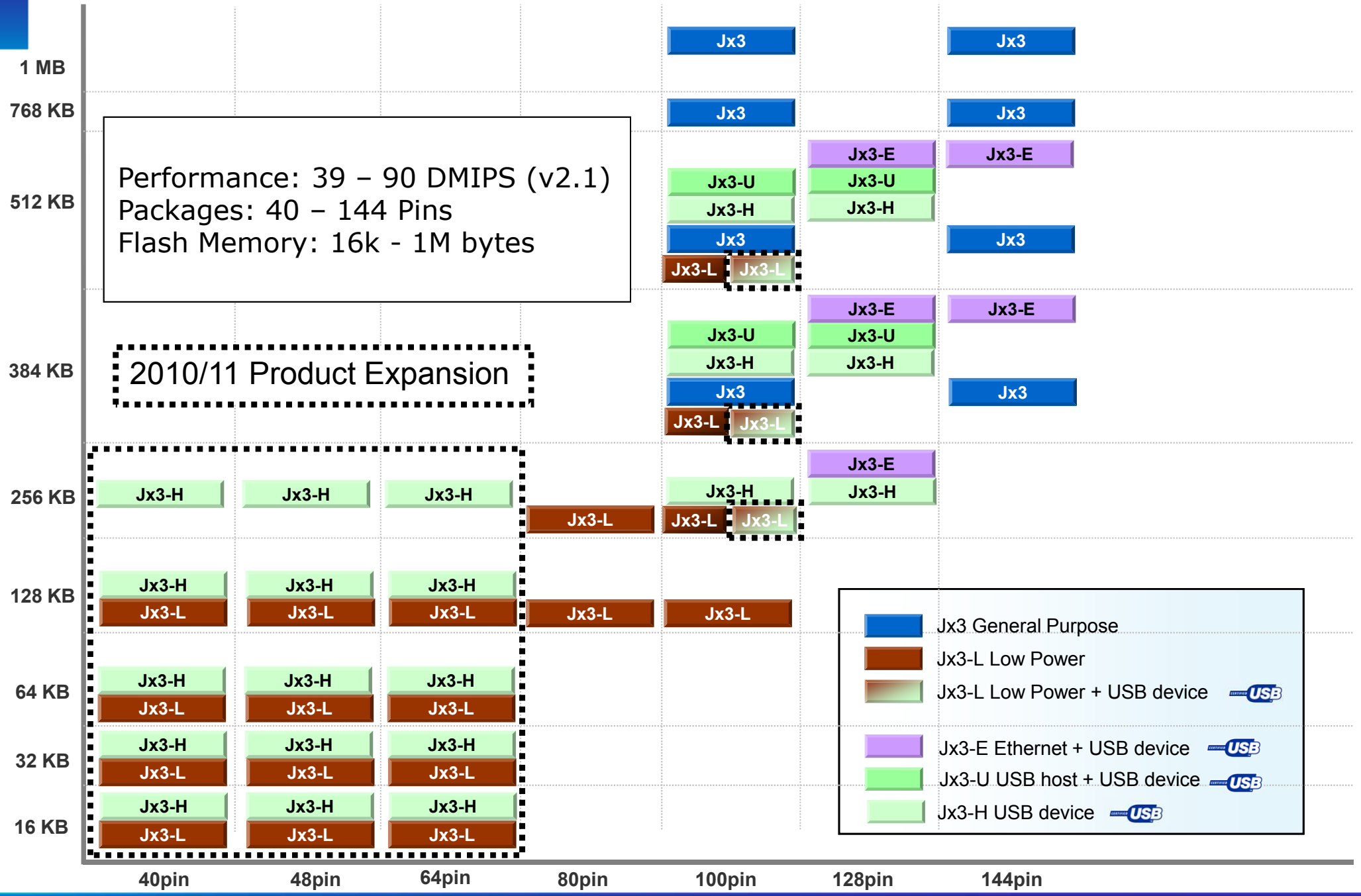
Scalable Family to Meet Different Cost Structure



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Thank You

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